# PXIe-4162 Specifications



2025-04-28

# Contents

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## PXIe-4162 Specifications

These specifications apply to the PXIe-4162.

**Note** In this document, the PXIe-4162 (10 pA) and PXIe-4162 (100 pA) are referred to inclusively as the PXIe-4162.

The information in this document applies to all versions of the PXIe-4162 unless otherwise specified. Use the information in the following table to confirm your module variant.

Table 5. PXIe-4162 Variant Identification

| Model | Location | Identifying Information |
|---|---|---|
| PXIe-4162 (10 pA) | NI Measurement & Automation Explorer (MAX) | PXIe-4162 (10 pA) |
| | Device Front Panel | PXIe-4162 12-CH 10pA SMU |
| PXIe-4162 (100 pA) | NI Measurement & Automation Explorer (MAX) | PXIe-4162 |
| | Device Front Panel | PXIe-4162 12-CH Precision SMU |

## Looking For Something Else?

For information not found in the specifications for your product, such as operating instructions, browse *Related Information*.

**Related information:**

- PXIe-4162 User Manual

- NI-DCPower User Manual

## Definitions

*Warranted Specifications* describe the performance of a model under stated operating conditions and are covered by the model warranty.

*Characteristics* describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical**—describes the performance met by a majority of models.
- **Typical-95**—describes the performance met by 95% (≈2σ) of models with a 95% confidence.
- **Nominal**—describes an attribute that is based on design, conformance testing, or supplemental testing.

Values are *Nominal* unless otherwise noted.

## Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature[1] of 23 °C ± 5 °C
- Chassis with slot cooling capacity ≥38 W[2]
  - For chassis with slot cooling capacity = 38 W, fan speed set to HIGH
- Calibration interval of 1 year
- 30 minutes warm-up time
- Self-calibration performed within the last 24 hours
- NI-DCPower Aperture Time is set to 2 power-line cycles (PLC)

## PXIe-4162 Pinout

The following figure shows the terminals on the PXIe-4162 connector.

1. The ambient temperature of a PXI system is defined as the temperature at the chassis fan inlet (air intake).
2. For increased capability, NI recommends installing the PXIe-4162 in a chassis with slot cooling capacity ≥58 W.

Figure 1. PXIe-4162 Connector Pinout

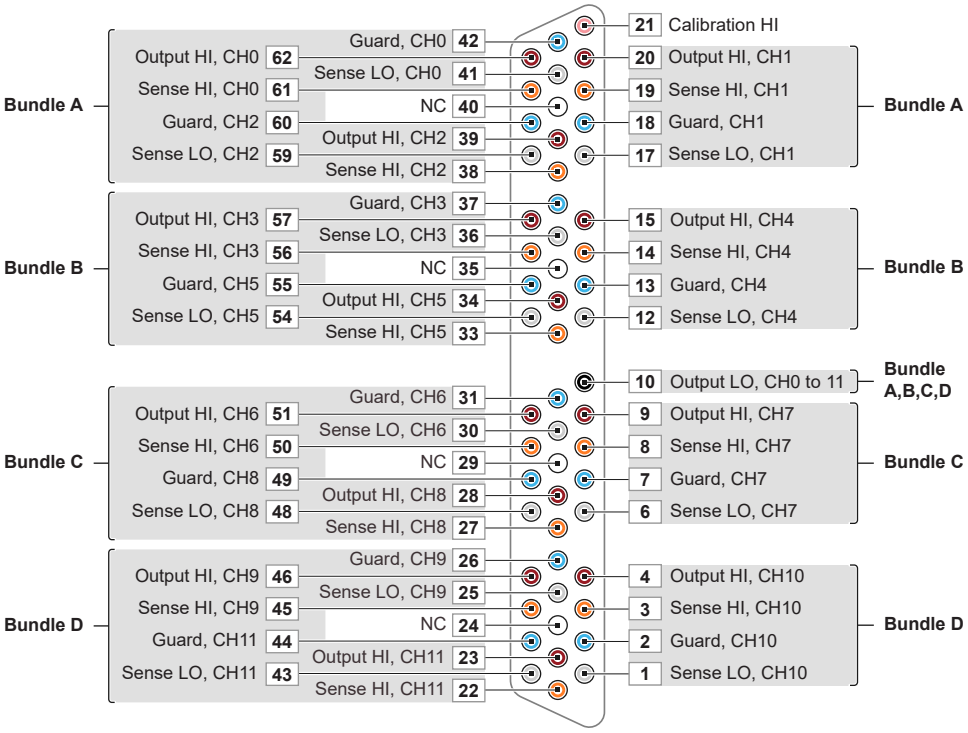



Table 6. Signal Descriptions

| Signal Name | Description |
|---|---|
| CH <0..11> Sense LO | Voltage remote sense input terminals. Used to compensate for *I*R* voltage drops in cable leads, connectors, and switches. |
| CH <0..11> Guard | Buffered output that follows the voltage of the HI force terminal. Used to drive shield conductors surrounding HI force and Sense HI conductors to minimize effects of leakage and capacitance on low level currents. |
| CH <0..11> Sense HI | Voltage remote sense input terminals. Used to compensate for *I*R* voltage drops in cable leads, connectors, and switches. |
| CH <0..11> Output HI | HI force terminal connected to channel power stage (generates and/or dissipates power). Positive polarity is defined as voltage measured on HI > LO. |
| CH <0..11> Output LO | LO force terminal connected to channel power stage (generates and/or dissipates power). Positive polarity is defined as voltage measured |

| Signal Name | Description |
|---|---|
| | on HI > LO. |
| Calibration HI | For external calibration use only, otherwise leave unconnected. |
| NC | No Connect. |

**Note** Guard terminals are not supported in the highest current ranges: 60 mA or 100 mA.

**Note** The PXIe-4162 has 12 channels organized into four cable bundles (A, B, C, D) for use with associated cable accessories.

# Instrument Capabilities

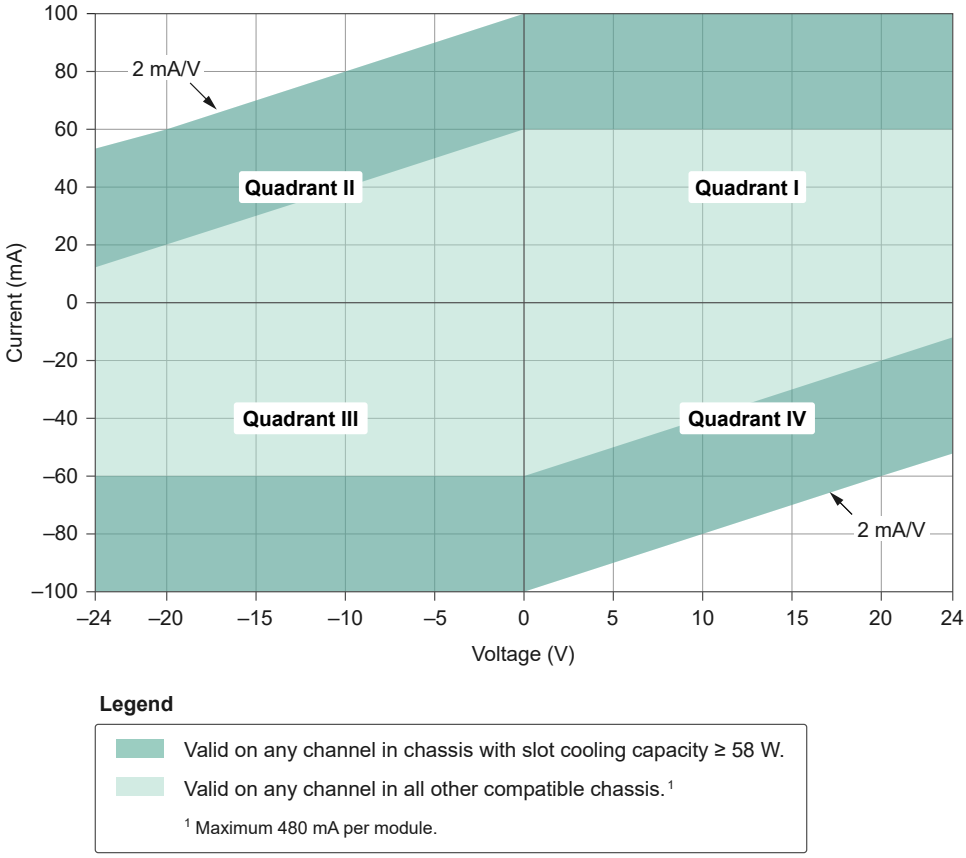
| | |
|---|---|
| Channels | 0 through 11 |
| DC voltage range | ±24 V |

The following table and figure illustrate the voltage and the current source and sink ranges of the PXIe-4162.

Table 7. PXIe-4162 DC Current Source and Sink Ranges, Warranted

| Device Model | Chassis Slot Cooling Capacity ≥58 W | Chassis Slot Cooling Capacity 38 W |
|---|---|---|
| PXIe-4162 (10 pA) only | 1 µA | 1 µA |
| All PXIe-4162 models | 10 µA | 10 µA |
| All PXIe-4162 models | 100 µA | 100 µA |
| All PXIe-4162 models | 1 mA | 1 mA |
| All PXIe-4162 models | 10 mA | 10 mA |
| All PXIe-4162 models | 100 mA | 60 mA |

Figure 2. PXIe-4162 Quadrant Diagram, Any Channel




# Voltage

Table 8. Voltage Programming and Measurement Accuracy/Resolution, Warranted

| Range | Resolution and Noise (0.1 Hz to 10 Hz, peak-to-peak, typical) | Accuracy (23 °C ± 5 °C) ± (% of Voltage + Offset) [3] $T_{cal}$ ± 5 °C | Tempco [4] ± (% of Voltage + Offset)/°C, 0 °C to 55 °C |
|---|---|---|---|
| 24 V | 200 µV | 0.05% + 5 mV | 0.0005% + 1 µV |

3. Refer to remote sense and load regulation sections for additional accuracy derating and conditions.
4. Temperature coefficient applies beyond 23 °C ± 5 °C within 5 °C of $T_{cal}$.

# Current

Table 9. PXIe-4162 (10 pA) Current Programming and Measurement Accuracy/Resolution, Warranted

| Range | Resolution and Noise (0.1 Hz to 10 Hz, peak-to-peak, typical) | Accuracy (23 °C ± 5 °C) ± (% of Current + Offset)[5] $T_{cal}$ ± 5 °C | Tempco[6] ± (% of Current + Offset)/°C, 0 °C to 55 °C |
|---|---|---|---|
| 1 µA | 10 pA | 0.10% + 100 pA | 0.004% + 20 pA |
| 10 µA | 100 pA | 0.10% + 1 nA | 0.004% + 20 pA |
| 100 µA | 1 nA | 0.10% + 10 nA | 0.004% + 100 pA |
| 1 mA | 10 nA | 0.10% + 100 nA | 0.004% + 1 nA |
| 10 mA | 100 nA | 0.10% + 1 µA | 0.004% + 10 nA |
| 60 mA or 100 mA[7] | 1 µA | 0.10% + 10 µA | 0.004% + 100 nA |

Table 10. PXIe-4162 (100 pA) Current Programming and Measurement Accuracy/Resolution, Warranted

| Range | Resolution and Noise (0.1 Hz to 10 Hz, peak-to-peak, typical) [8] | Accuracy (23 °C ± 5 °C) ± (% of Current + Offset)[9] $T_{cal}$ ± 5 °C | Tempco[10] ± (% of Current + Offset)/°C, 0 °C to 55 °C |
|---|---|---|---|
| 10 µA | 100 pA | 0.10% + 5 nA | 0.004% + 10 pA |
| 100 µA | 1 nA | 0.10% + 50 nA | 0.004% + 100 pA |
| 1 mA | 10 nA | 0.10% + 500 nA | 0.004% + 1 nA |

5. Refer to remote sense and load regulation sections for additional accuracy derating and conditions.
6. Temperature coefficient applies beyond 23 °C ± 5 °C within 5 °C of $T_{cal}$.
7. 100 mA range available only when installed in chassis with slot cooling capacity ≥58 W. 60 mA range available in all other compatible chassis.
8. Specified values apply for $V_{output\ HI}$ ≤5 V; add 0.0002% of range per volt above 5 V .
9. Refer to remote sense and load regulation sections for additional accuracy derating and conditions.
10. Temperature coefficient applies beyond 23 °C ± 5 °C within 5 °C of $T_{cal}$.

| Range | Resolution and Noise (0.1 Hz to 10 Hz, peak-to-peak, typical) | Accuracy (23 °C ± 5 °C) ± (% of Current + Offset)<br><br>$T_{cal}$ ± 5 °C | Tempco ± (% of Current + Offset)/°C, 0 °C to 55 °C |
|---|---|---|---|
| 10 mA | 100 nA | 0.10% + 5 µA | 0.004% + 10 nA |
| 60 mA or 100 mA[11] | 1 µA | 0.10% + 50 µA | 0.004% + 100 nA |

**Note** For more information about the impact to specifications when using NI-DCPower Merged Channels, refer to *Effect of Merging Channels on Performance Specifications* in the PXIe-4162 User Manual.

**Related information:**

- Effect of Merging Channels on Performance Specifications

# Available DC Output Power

| Chassis Slot Cooling Capacity | Per Channel Maximum | Absolute Maximum |
|---|---|---|
| ≥58 W | 2.4 W | 28.8 W |
| 38 W | 1.4 W | 11.5 W |

# Additional Specifications

Table 11. Dynamic Specifications

| | |
|---|---|
| Settling time[12] | <500 µs, typical[13] |
| Transient response[14] | <100 µs, typical[15] |

11. 100 mA range available only when installed in chassis with slot cooling capacity ≥58 W. 60 mA range available in all other compatible chassis.
12. Current limit set to ≥1 mA and ≥10% of the selected current limit range. PXIe-4162 configured for fast transient response.
13. To settle to 0.1% of voltage step.
14. PXIe-4162 configured for fast transient response.

| | |
|---|---|
| Wideband source noise[16] | 15 mV RMS, typical<br><100 mV, peak-to-peak, typical |

Table 12. Remote Sense

| | |
|---|---|
| Voltage | No additional error due to lead drop |
| Current | No additional error due to lead drop |
| Maximum lead drop | 1 V drop/lead |

Table 13. Load Regulation

| | |
|---|---|
| Voltage[17] | 50 µV/mA, typical |
| Current | (30 pA + 20 ppm of range)/volt, typical[18] |

Table 14. Electrical Safety Specifications

| | |
|---|---|
| Cable guard output current limit[19] | 100 µA |
| Isolation voltage, any pin to earth ground[20] | 60 V DC, Measurement Category I, functional |

Table 15. Absolute Maximum Voltage to Output LO

Conditions: Absolute maximum voltage Sense HI, Sense LO, or Guard measured where $V_{Output\ HI}$ is the voltage at the Output HI pin in the same channel as a Sense HI, Sense LO, or Guard pin.

| | |
|---|---|
| From Sense HI, Sense LO, or Guard when | -0.5 V to ($V_{Output\ HI}$ + 0.5 V) |

15. To recover within ±20 mV after a load current change from 10% to 90% of range.
16. 20 Hz to 20 MHz bandwidth. PXIe-4162 configured for normal transient response. Measured at the end of the 1 m SHDB62M-DB62M-LL cable.
17. At connector pins when using local sense.
18. For more information about the impact to specifications when using NI-DCPower Merged Channels, refer to *Effect of Merging Channels on Performance Specifications* in the PXIe-4162 User Manual.
19. At current ranges ≥60 mA guard outputs are disabled and are high-impedance.
20. Pins are functionally isolated from chassis ground to prevent ground loops, but do not meet IEC 61010-1 for safety isolation.

| | |
|---|---|
| $V_{Output\ HI} > 0$ V | |
| From Sense HI, Sense LO, or Guard when $V_{Output\ HI} \leq 0$ V | ($V_{Output\ HI}$ - 0.5 V) to 0.5 V |
| From all other pins | ±25 V |

**Notice** Avoid connecting the PXIe-4162 output to a voltage that deviates by more than ±2.5 V from the actual CHx Output HI voltage. When determining this voltage difference, be sure to consider the setpoint, settling, **Output Enabled** status, **Output Connected** status, and compliance. For for more information, refer to *Performing Voltage and Current Measurements with the PXIe-4162* in the PXIe-4162 User Manual.

**Notice** Exceeding the absolute maximum voltage from Sense HI to Output LO when using remote sense can result in a Remote Sense OVP Error in NI-DCPower 23.0 and later.

**Related information:**

- Performing Voltage and Current Measurements with the PXIe-4162

## Noise versus Aperture Time

The following figures illustrate noise as a function of measurement aperture for the PXIe-4162.

Figure 3. Voltage RMS Noise versus Aperture Time[21]

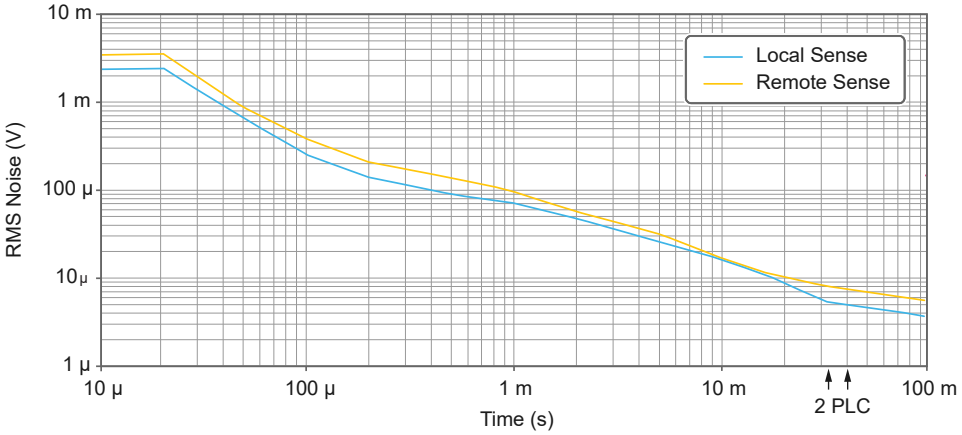
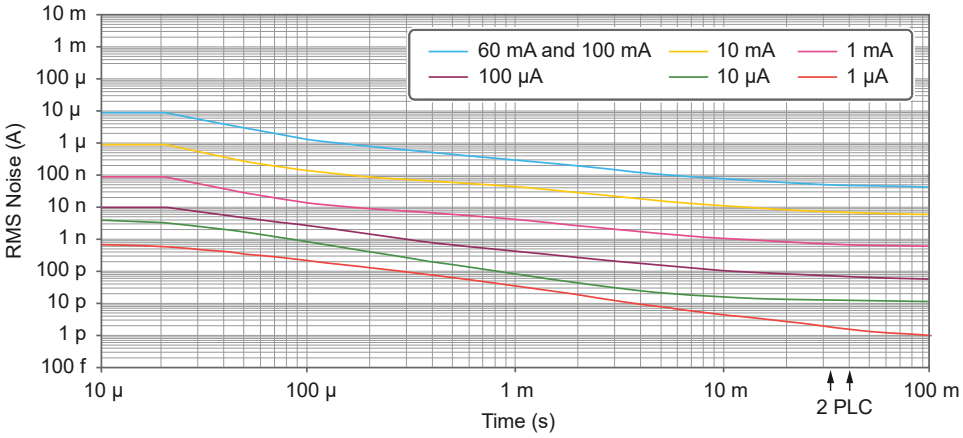



Figure 4. Current RMS Noise versus Aperture Time[22, 23]




**Note** When the aperture time is set to two power-line cycles (PLCs), measurement noise differs slightly depending on whether the NI-DCPower Power Line Frequency is set to `50 Hertz` or `60 Hertz`.

**Note** To configure DC Noise rejection, set the NI-DCPower DC Noise Rejection to `Normal` or `Second-Order`.

**Note** For more information about the impact to specifications when using NI-DCPower Merged Channels, refer to *Effect of Merging Channels on Performance Specifications* in the PXIe-4162 User Manual.

**Related information:**

21. All channels averaged. Channel 11 has degraded performance.
22. The 1 µA range applies only to the PXIe-4162 (10 pA).
23. All channels averaged. In the 100 mA range, channel 4 has degraded performance.

- Effect of Merging Channels on Performance Specifications

# Measurement and Update Timing

Table 16. Sample Rate Specifications

| | |
|---|---|
| Available sample rates[24] | (600 kS/s)/N<br><br>where<br><br>• N = 6, 7, 8, … $2^{20}$<br>• S is samples |
| Sample rate accuracy | ±50 ppm |
| Maximum measure rate to host[25] | 100,000 S/s per channel, continuous |

Table 17. Maximum Source Update Rate

**Note** As the source delay is adjusted or if advanced sequencing is used, maximum source update rates may vary.

| | |
|---|---|
| Single channel | 100,000 updates/s |
| All channels simultaneously | 40,000 updates/s per channel |

Table 18. Input Trigger to

| | |
|---|---|
| Source event delay | 8.5 µs |
| Source event jitter | 1.7 µs |
| Measure event jitter | 1.7 µs |

24. When source-measuring, both the NI-DCPower Source Delay and Aperture Time properties affect the sampling rate. When taking a measure record, only the Aperture Time property affects the sampling rate.
25. Load dependent settling time is not included. Normal DC noise rejection is used.

# Triggers

**Note** Pulse widths and logic levels for PXI trigger lines 0 to 7 are compliant with *PXI Express Hardware Specification Revision 1.0 ECN 1*.

## Input Triggers

Table 19. Input Trigger Types

| | |
|---|---|
| Types | Start<br>Source<br>Sequence Advance<br>Measure |

Table 20. Input Trigger Sources (PXI trigger lines 0 to 7)

| | |
|---|---|
| Polarity | Active high (not configurable) |
| Minimum pulse width | 100 ns |

Table 21. Input Trigger Destinations (PXI trigger lines 0 to 7)

| | |
|---|---|
| Polarity | Active high (not configurable) |
| Minimum pulse width | >200 ns |

**Note** Input triggers can come from any source (PXI trigger or software trigger) and be exported to any PXI trigger line. This allows for easier multi-board synchronization regardless of the trigger source.

## Output Triggers (Events)

Table 22. Output Trigger Types

| | |
|---|---|
| Types | Source Complete |

| | |
|---|---|
| | Sequence Iteration Complete<br>Sequence Engine Done<br>Measure Complete |

Table 23. Output Trigger Destinations (PXI trigger lines 0 to 7)

| | |
|---|---|
| Polarity | Active high (not configurable) |
| Pulse width | 230 ns |

# Power Requirements

Table 24. 38 W Chassis Slot Cooling Capacity

| Power Rail | State | Power Requirement |
|---|---|---|
| +3.3 V Current Draw, Typical | Idle | 1 A |
| +3.3 V Current Draw, Typical | Full Output Load | 1 A |
| +12 V Current Draw, Typical | Idle | 1.5 A |
| +12 V Current Draw, Typical | Full Output Load | 3 A |

Table 25. ≥58 W Chassis Slot Cooling Capacity

| Power Rail | State | Power Requirement |
|---|---|---|
| +3.3 V Current Draw, Typical | Idle | 1 A |
| +3.3 V Current Draw, Typical | Full Output Load | 1 A |

| Power Rail | State | Power Requirement |
|---|---|---|
| +12 V Current Draw, Typical | Idle | 1.5 A |
| +12 V Current Draw, Typical | Full Output Load | 4.5 A |

## Physical

| | |
|---|---|
| Dimensions | 3U, one-slot, PXI Express/CompactPCI Express module<br><br>2.1 cm × 13.1 cm × 21.4 cm<br>(0.8 in. × 5.1 in. × 8.4 in.)<br><br>For more information, visit *ni.com/dimensions* and search by module number. |
| Weight | 394 g (13.9 oz) |
| Front panel connector | Custom 62-position D-SUB, female |

## Environmental Guidelines

**Notice** Failure to follow the mounting instructions in the product documentation can cause temperature derating.

**Notice** This product is intended for use in indoor applications only.

## Environmental Characteristics

Table 26. Temperature

| | |
|---|---|
| Operating temperature for chassis with slot cooling capacity ≥58 W[26] | 0 °C to 55 °C |

26. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to

| | |
|---|---|
| Operating temperature for all other compatible chassis | 0 °C to 40 °C |
| Storage | -40 °C to 71 °C |

Table 27. Humidity

| | |
|---|---|
| Operating | 10% to 90%, noncondensing |
| Storage | 5% to 95%, noncondensing |

Table 28. Pollution Degree

| | |
|---|---|
| Pollution degree | 2 |

Table 29. Maximum Altitude

| | |
|---|---|
| Maximum altitude | 2,000 m (800 mbar) (at 25 °C ambient temperature) |

Table 30. Shock and Vibration

| | |
|---|---|
| Operating vibration | 5 Hz to 500 Hz, 0.3 g RMS |
| Non-operating vibration | 5 Hz to 500 Hz, 2.4 g RMS |
| Operating shock | 30 g, half-sine, 11 ms pulse |

# Calibration Interval

You can obtain the calibration certificate and information about calibration services for the PXIe-4162 at ni.com/calibration.

Table 31. Calibration Interval

| | |
|---|---|
| Calibration Interval | 1 year |

PXI chassis specifications to determine the ambient temperature ranges your chassis can achieve.