
PXIe-7971

Specifications



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These specifications apply to the PXle-7971.

Definitions

Warranted Specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

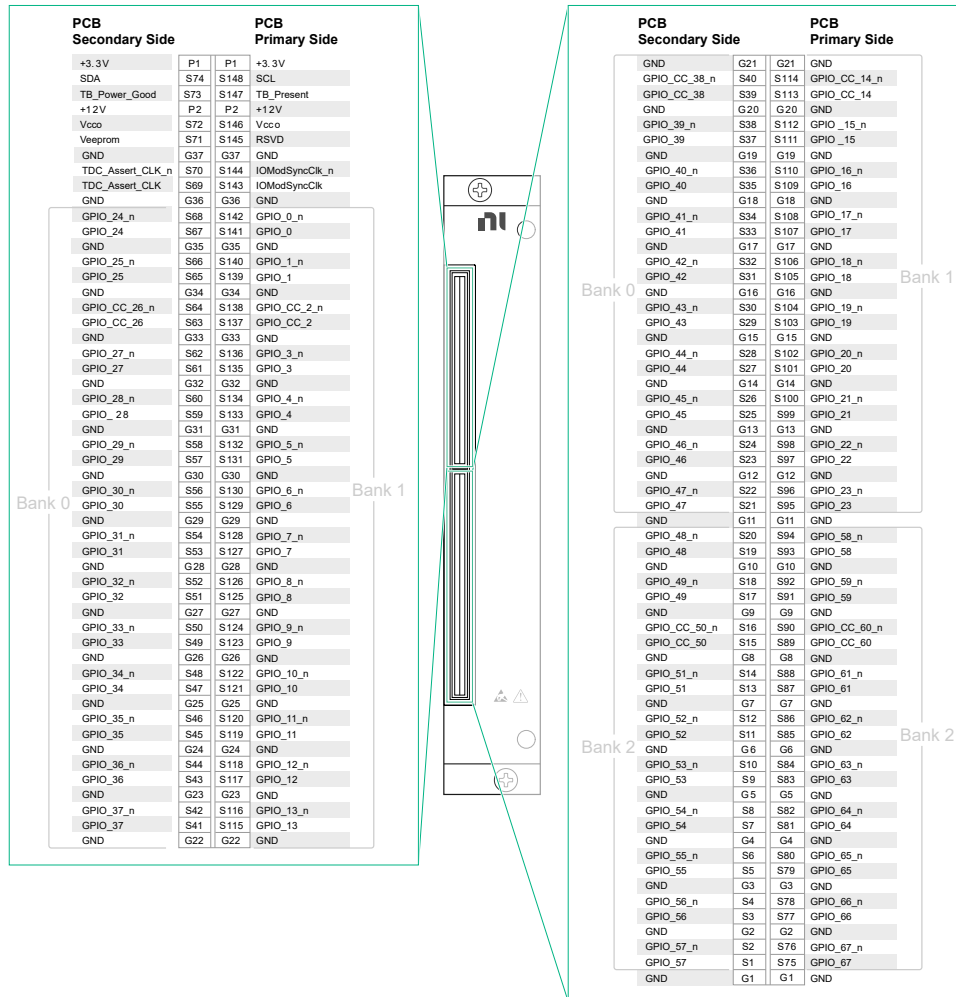
- **Typical**—describes the performance met by a majority of models.
- **Nominal**—describes an attribute that is based on design, conformance testing, or supplemental testing.

Values are ***Typical*** unless otherwise noted.

PXle-7971 Pinout

Use the pinout to connect to terminals on the PXle-7971.

Figure 1. PXle-7971 Connector Pinout



Pins S72 and S146 are shorted together.

Reconfigurable FPGA

Table 1. Reconfigurable FPGA

Specification	Value
FPGA	Kintex-7 XC7K325T
LUTs	203,800
DSP48 Slices (25 × 18 Multiplier)	840
Embedded Block RAM (kbits)	16,020
Default timebase	40 MHz
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)

Specification	Value
Timebase accuracy	± 100 ppm, 250 ps peak-to-peak jitter
Data transfers	DMA, interrupts, programmed I/O
Number of DMA channels	32

FPGA Digital Input/Output

Table 2. FPGA Digital Input/Output

Specification	Value
Number of general-purpose channels	136, configurable as 136 single-ended, 68 differential, or a combination of both ¹
Compatibility	Configured through the FPGA and based on the attached adapter module; 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V I/O standards (refer to xilinx.com).
Protection	Refer to xilinx.com .
Current	Refer to xilinx.com .
Multi-region clock inputs	6
Single-region clock inputs	5
Connection resources	PXI triggers, PXI_CLK10, PXI star trigger, PXIe_DStarA, PXIe_DStarB, PXIe_DStarC, and PXIe_Sync100

Table 3. Channels per Bank

Specification	Value
Bank 0/Bank 1	48
Bank 2	40

Table 4. Maximum I/O Data Rates

Specification	Value
Single-ended	400 Mb/s
Differential	1 Gb/s for LVDS

1. The 136 channels span across three FPGA banks.

Bus Interface

Table 5. Bus Interface

Specification	Value
Form factor	x4 PXI Express, specification v2.1 compliant
Slot compatibility	x4, x8, and x16 PXI Express or PXI Express hybrid slots

Maximum Power Requirements



Note Power requirements are dependent on the adapter module and contents of the LabVIEW FPGA VI used in your application.

Table 6. Maximum Power Requirements

Specification	Value
+3.3 VDC ($\pm 5\%$)	3 A
+12 V	3 A

Physical

Table 7. Physical Characteristics

Dimensions (not including connectors)	18.8 cm × 12.9 cm (7.4 in. × 5.1 in.) For more information, visit ni.com/dimensions and search by module number.
Weight	190 g (6.7 oz)

Maximum Working Voltage



Note Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Table 8. Maximum Working Voltage

Specification	Value
Channel-to-earth	0 V to 3.3 V, Measurement Category I
Channel-to-channel	0 V to 3.3 V, Measurement Category I



Caution Do not use this device for connecting to signals in Measurement Categories II, III, or IV.

Environmental Characteristics

Table 9. Temperature

Characteristic	Specification
Operating temperature	0 °C to 55 °C
Storage temperature	-20 °C to 70 °C

Table 10. Humidity

Characteristic	Specification
Operating humidity	10% to 90%, noncondensing
Storage humidity	5% to 95%, noncondensing

Table 11. Pollution Degree

Characteristic	Specification
Pollution Degree	2

Table 12. Maximum Altitude

Characteristic	Specification
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)

Table 13. Shock and Vibration

Characteristic	Specification
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse