SPECIFICATIONS

PXIe-6594

28 Gbps, 8-Channel PXI High-Speed Serial Instrument

Contents

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured* specifications describe the measured performance of a representative model.

Specifications are *Typical* unless otherwise noted.

NATIONAL INSTRUMENTS

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 0 °C to 55 °C
- Installed in chassis with slot cooling capacity ≥58 W

PORT 0, PORT 1

Data rate	500 Mb/s to 28.2 Gb/s
Connector	QSFP, SFF-8436 compliant
Number of channels	8 RX/TX (GTY)
Supported high-speed cable type	Electrical/optical
Optical cable power	3.3 V ±5%, 1 A per port

MGT TX± Channels

Minimum differential output voltage[1]	170 mV pk-pk into 100 Ω, nominal
I/O coupling	AC-coupled, includes 100 nF capacitor

MGT RX± Channels

Differential input voltage range	
≤ 6.6 Gb/s	150 mV pk-pk to 2000 mV pk-pk, nominal
> 6.6 Gb/s	150 mV pk-pk to 1250 mV pk-pk, nominal
Differential input resistance	100 Ω, nominal
I/O coupling	DC-coupled, requires external capacitor

MGT Reference Clock Generator

Generated frequency	
Range	60 MHz to 800 MHz
Gaps	385.714 MHz < freq < 400.000 MHz 450.000 MHz < freq < 480.000 MHz 675.000 MHz < freq < 685.714 MHz 771.428 MHz < freq < 800.000 MHz

[1] 800 mV pk-pk when transmitter output swing is set to the maximum setting.

Locking resources	PXIe_CLK100 REF/CLK IN
Available MGT Reference Clocks	4

CLK OUT

Connector type	SMA
Coupling	AC
Output impedance	50 Ω, nominal
Supported output frequencies	2.344 MHz to 385.714 MHz 400.000 MHz to 450.000 MHz 480.000 MHz to 675.000 MHz 685.714 MHZ to 771.428 MHz 800.000 MHz to 900.000 MHz 960.000 MHz to 1000.000 MHz
Output voltage range	0.61 V pk-pk to 1.04 V pk-pk

REF/CLK IN

Connector type	SMA
Input coupling	AC
Input impedance	50 Ω
Frequency range	10 MHz to 300 MHz
Input voltage range	0.3 V pk-pk to 4 V pk-pk
Absolute maximum voltage	5 V pk-pk AC
Duty cycle	45% to 55%

DIO

Connector	Molex™ Nano-Pitch I/O™
5.0 V Power	±5%, 50 mA maximum, nominal

Table 1. Digital I/O Signal Characteristics

Signal	Type	Direction
MGT Tx± <0..3>	Xilinx UltraScale+ GTY	Output
MGT Rx± <0..3>	Xilinx UltraScale+ GTY	Input
DIO <0..7>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

Digital I/O Single-Ended Channels

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 kΩ, nominal
Output impedance	50 Ω, nominal
Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 µA load, nominal

Table 2. Digital I/O Single-Ended DC Signal Characteristics[2]

Voltage Family	V_{IL}	V_{IH}	V_{OL} (100µA load)	V_{OH} (100µA load)	Maximum DC Drive Strength
3.3 V	0.8 V	2.0 V	0.2 V	3.0 V	24 mA
2.5 V	0.7 V	1.6 V	0.2 V	2.2 V	18 mA
1.8 V	0.62 V	1.29 V	0.2 V	1.5 V	16 mA
1.5 V	0.51 V	1.07 V	0.2 V	1.2 V	12 mA
1.2 V	0.42 V	0.87 V	0.2 V	0.9 V	6 mA

[2] Voltage levels are guaranteed by design through the digital buffer specifications.

Digital I/O High-Speed Serial MGT[3]

Data rate	500 Mb/s to 16.375 Gb/s, nominal
Number of Tx channels	4
Number of Rx channels	4
I/O coupling	
MGT TX± Channels	AC-coupled, includes 100 nF capacitor
MGT RX± Channels	DC-coupled, requires external capacitor

Reconfigurable FPGA

Kintex Ultrascale+	15P
LUTs	523,000
DSP48 slices (25 × 18 multiplier)	1,968
Embedded Block RAM	34.6
Timebase reference sources	PXI Express 100 MHz (PXI_CLK100)
Data transfers	DMA, interrupts, programmed I/O, MGTs
Number of DMA channels	60

Onboard DRAM

Memory size	8 GB (2 banks of 4 GB)
DRAM clock rate	1333 MHz
Physical bus width	64 bit
LabVIEW FPGA DRAM clock rate	333 MHz
LabVIEW FPGA DRAM bus width	512 bits per bank
Maximum theoretical data rate	42.7 GB/s (21.3 GB/s per bank)

Bus Interface

Form factor	PCI Express Gen-3 x8

[3] For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

Maximum Power Requirements

Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	3 A
+12 V	4 A
Maximum total power	58 W

Physical

Dimensions (not including connectors)	2.0 cm × 13.0 cm × 21.6 cm (0.8 in. × 5.1 in. × 8.5 in.)
Weight	520 g (18.3 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C[4]
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-40 °C to 71 °C
Relative humidity range	5% to 95%, noncondensing

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse

[4] The PXIe-6594 requires a chassis with slot cooling capacity ≥58 W. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to the *PXI Chassis Manual* for specifications to determine the ambient temperature ranges your chassis can achieve.

Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms}

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