PXIe-5785 Specifications

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Contents

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Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured* specifications describe the measured performance of a representative model.

Specifications are *Typical* unless otherwise noted.

PXIe-5785 Pinout

Use the pinout to connect to terminals on the PXIe-5785.

Figure 1. PXIe-5785 Digital I/O Connector Pinout

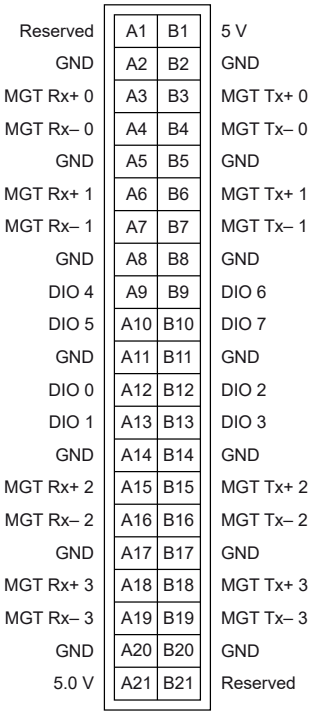


Table 1. PXIe-5785 Digital I/O Connector Signal Descriptions

Signal	Type	Direction
MGT Tx± <0..3>	Xilinx UltraScale GTH	Output
MGT Rx± <0..3>	Xilinx UltraScale GTH	Input
DIO <0..7>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

Notice The maximum input signal levels are valid only when the module is powered on. To avoid permanent damage to the PXIe-5785, do not apply a signal to the device when the module is powered down.

Notice Connections that exceed any of the maximum ratings of any connector on the PXIe-5785 can damage the device and the system. NI is not liable for any damage resulting from such connections.

Note MGTs are available only on devices with KU040 and KU060 FPGAs.

Digital I/O

Connector	Molex™ Nano-Pitch I/O™
5.0 V Power	±5%, 50 mA maximum, nominal

Table 2. Digital I/O Signal Characteristics

Signal	Type	Direction
MGT Tx± <0..3>[1]	Xilinx UltraScale GTH	Output
MGT Rx± <0..3>[1]	Xilinx UltraScale GTH	Input
DIO <0..7>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

Digital I/O Single-Ended Channels

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 kΩ, nominal

1. Multi-gigabit transceiver (MGT) signals are available on devices with KU040 and KU060 FPGAs only.

Output impedance	50 Ω, nominal
Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 µA load, nominal

Table 3. Digital I/O Single-Ended DC Signal Characteristics[2]

Voltage Family (V)	V_{IL} (V)	V_{IH} (V)	V_{OL} (100 µA Load) (V)	V_{OH} (100 µA Load) (V)	Maximum DC Drive Strength (mA)
3.3	0.8	2.0	0.2	3.0	24
2.5	0.7	1.6	0.2	2.2	18
1.8	0.62	1.29	0.2	1.5	16
1.5	0.51	1.07	0.2	1.2	12
1.2	0.42	0.87	0.2	0.9	6

Digital I/O High-Speed Serial MGT[3]

Note MGTs are available on devices with KU040 and KU060 FPGAs only.

Data rate	500 Mbps to 16.375 Gbps, nominal
Number of Tx channels	4

2. Voltage levels are guaranteed by design through the digital buffer specifications.
3. For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

Number of Rx channels	4
I/O AC coupling capacitor	100 nF

Reconfigurable FPGA

PXIe-5785 modules are available with multiple FPGA options. The following table lists the FPGA specifications for the PXIe-5785 FPGA options.

Table 4. Reconfigurable FPGA Options

	KU035	KU040	KU060
LUTs	203,128	242,200	331,680
DSP48 slices (25 × 18 multiplier)	1,700	1,920	2,760
Embedded Block RAM	19.0 Mb	21.1 Mb	38.0 Mb
Data Clock Domain	200 MHz, 16 samples per cycle per channel (dual channel mode), 32 samples per cycle (single channel mode)		
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)		
Data transfers	DMA, interrupts, programmed I/O	DMA, interrupts, programmed I/O, multi-gigabit transceivers	
Number of DMA channels	59		

Note The Reconfigurable FPGA Options table depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Analog Input

General Characteristics

Number of channels	2, single-ended, simultaneously sampled
Connector type	SMA
Input impedance	50 Ω
Input coupling	AC
Sample Clock	

Internal Sample Clock	3.2 GHz
External Sample Clock	2.8 GHz to 3.2 GHz
Sample Rate	
Dual channel mode	3.2 GS/s per channel
Single channel mode	6.4 GS/s
Analog-to-digital converter (ADC)	ADC12DJ3200, 12-bit resolution
Input latency[4]	239 ns

Typical Specifications

Full-scale input range	1.25 V pk-pk (5.92 dBm) at 10 MHz
AC gain accuracy	±0.11 dB at 10 MHz
DC offset	±2.19 mV
Bandwidth (-3 dB)[5]	500 kHz to 6 GHz

4. SMA input to LabVIEW diagram
5. Normalized to 10 MHz.

Table 5. Single-Tone Spectral Performance, Dual Channel Mode

	Input Frequency				
	99.9 MHz	**399 MHz**	**999 MHz**	**1.999 GHz**	**2.499 GHz**
SNR[6][] (dBFS)	56.0	55.6	54.7	52.9	51.6
SINAD[] (dBFS)	55.5	55.0	54.0	51.8	50.8
SFDR (dBc)	-64.9	-63.4	-62.7	-59.9	-58.6
ENOB[7][] (bits)	8.9	8.8	8.7	8.3	8.1

Table 6. Single-Tone Spectral Performance, Single Channel Mode[8]

	Input Frequency				
	99.9 MHz	**399 MHz**	**999 MHz**	**1.999 GHz**	**2.499 GHz**
SNR[] (dBFS)	54.6	54.2	52.4	49.7	48.9
SINAD[] (dBFS)	54.4	53.9	52.1	49.4	48.6
SFDR (dBc)	-61.7	-60.4	-56.1	-51.7	-51.1
ENOB[] (bits)	8.7	8.7	8.4	7.9	7.8

Table 7. Noise Spectral Density[9]

Mode	$\frac{nV}{\sqrt{Hz}}$	$\frac{dBm}{Hz}$	$\frac{dBFS}{Hz}$
Dual channel	14.4	-143.8	-149.2
Single channel	9.8	-147.2	-152.6

Note Noise spectral density is verified using a 50 Ω terminator connected to the input.

6. Measured with a -1 dBFS signal and corrected to full-scale. 3.2 kHz resolution bandwidth.
7. Calculated from SINAD and corrected to full scale.
8. Measured using channel AI0. Spectral performance may be degraded using channel AI1.
9. Excludes fixed interleaving spur (Fs/2 spur).

Figure 2. Single Tone Spectrum (Dual Channel Mode, 99.9 MHz, -1 dBFS, 3.2 kHz RBW), Measured

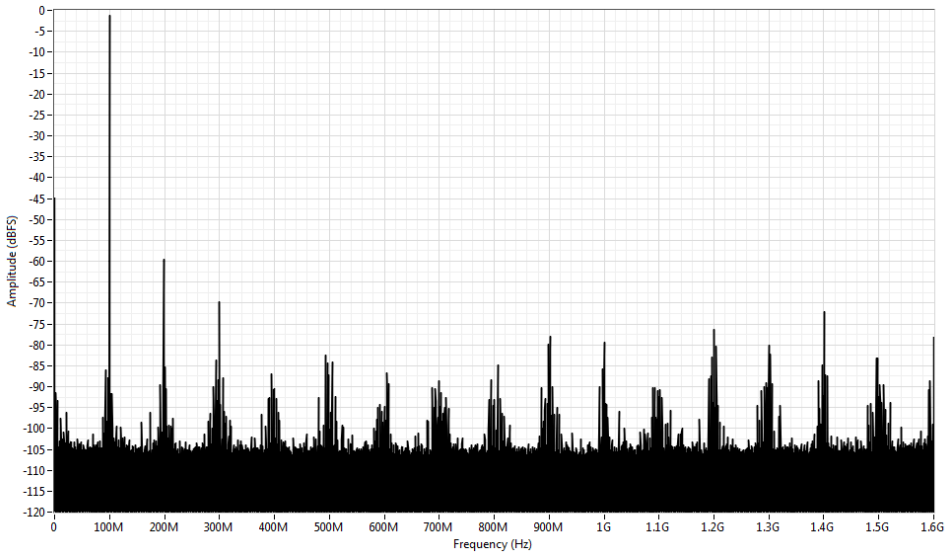


Figure 3. Single Tone Spectrum (Dual Channel Mode, 1.999 GHz, -1 dBFS, 3.2 kHz RBW), Measured

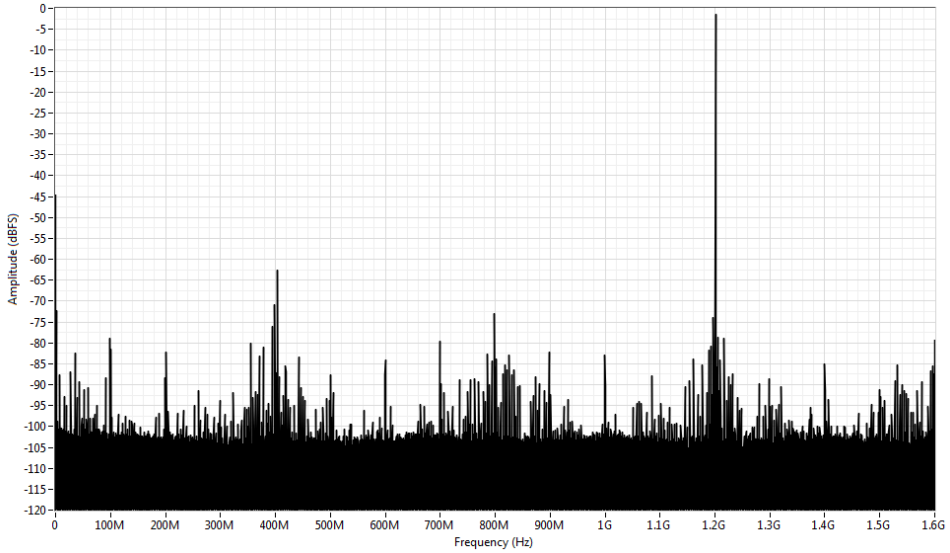


Figure 4. Single Tone Spectrum (Single Channel Mode, 99.9 MHz, -1 dBFS, 3.2 kHz RBW), Measured

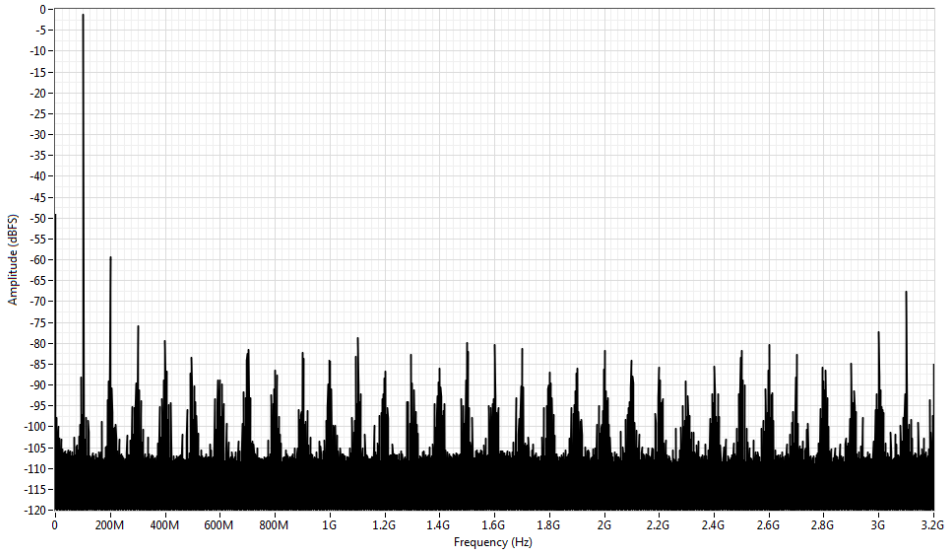
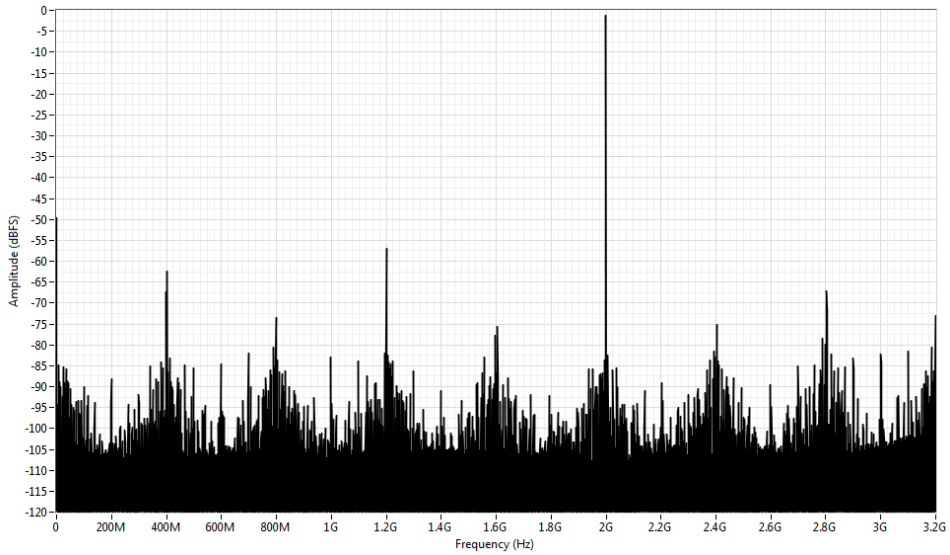


Figure 5. Single Tone Spectrum (Single Channel Mode, 1.999 GHz, -1 dBFS, 3.2 kHz RBW), Measured



Channel-to-channel crosstalk, measured	
99.9 MHz	-92.5 dB
399 MHz	-85.5 dB
999 MHz	-76.5 dB

1.999 GHz	-68.8 dB
2.499 GHz	-67.4 dB

Figure 6. Analog Input Frequency Response, Measured

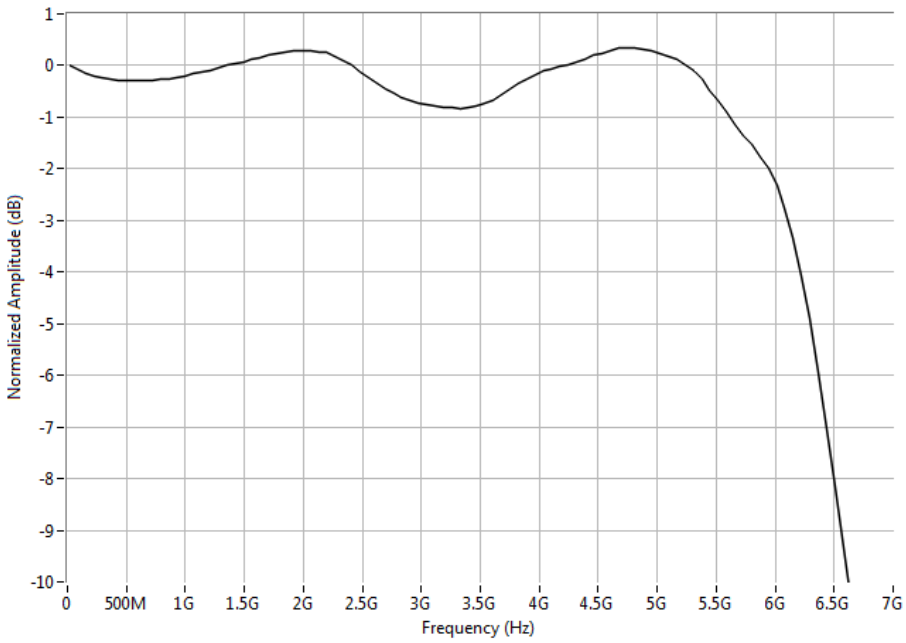
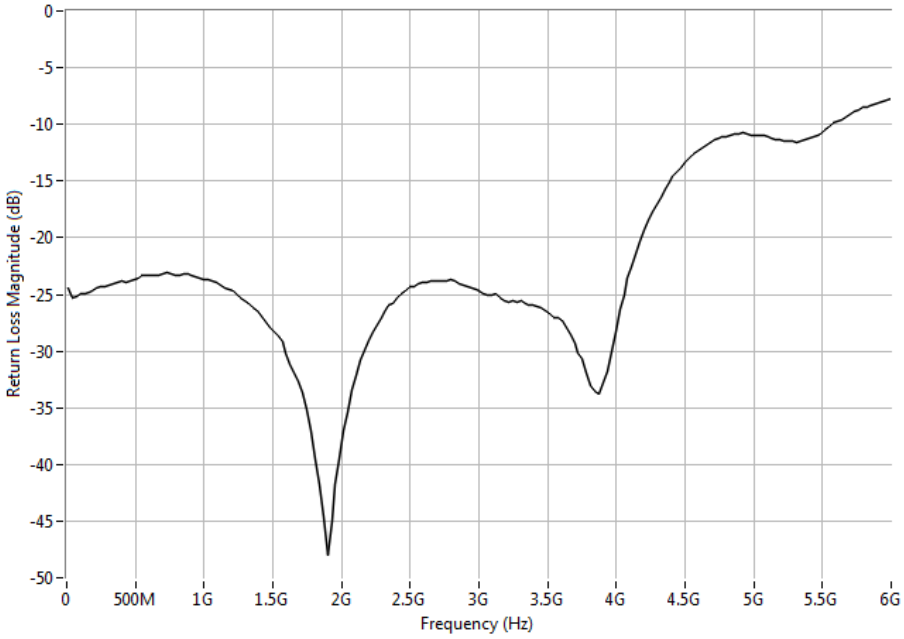


Figure 7. Input Return Loss, Measured



Analog Output

General Characteristics

Number of channels	2, single-ended, simultaneously updated
Connector type	SMA
Output impedance	50 Ω
Output coupling	AC
Update rate	
Internal Sample Clock, 2x interpolation	6.4 GS/s

External Sample Clock, 2x interpolation	6.4 GS/s [10]
Data rate (per channel)	
Dual channel mode	3.2 GS/s, real
Single channel mode	3.2 GS/s, complex
Digital-to-analog converter (DAC)	DAC38RF82, 12-bit resolution
Output latency[11]	
DUC disabled	211 ns
DUC enabled	221 ns

Typical Specifications

Note Due to a silicon flaw in the TI DAC38RF82 chip, there is a 0.5% chance of seeing a 50 mV glitch at the output of either channel after a bitfile re-download, invoking the Reset method explicitly or by closing the FPGA reference, or committing a new configuration.

Full-scale output power[12]	
Dual Channel Mode	2.85 dBm (878 mVpp)

10. To achieve this update rate when using an external sample clock, inject a 3.2 GS/s clock into the REF/CLK IN port and enable 2x interpolation.
11. LabVIEW diagram to SMA output
12. Into a 50 Ω load.

Single Channel Mode	-3.33 dBm (431 mVpp)
Bandwidth (-3 dB)[13]	
Dual Channel Mode	3 MHz to 1.53 GHz
Single Channel Mode (no anti-image filter)	60 MHz to 2.85 GHz
Single Channel Mode (with anti-image filter)	60 MHz to 2.35 GHz

Table 8. Single Tone Spectral Performance, Dual Channel Mode[14][]

	Generation Frequency	
	501 MHz	**1.01 GHz**
2nd HD (dBc)	-67.8	-61.7
3rd HD (dBc)	-63.0	-62.0
SFDR (dBc)	-63.0	-61.7

Table 9. Single Tone Spectral Performance, Single Channel Mode[]

	Generation Frequency
	1.01 GHz
2nd HD (dBc)	-62.4
3rd HD (dBc)	-67.3
SFDR (dBc)	-62.4

13. Normalized to 10 MHz in dual channel mode and 200 MHz in single channel mode. 2x interpolation and inverse sinc filter enabled.
14. DC, 3.2 GHz, output corrected to 0 dBFS by inverse sinc filter, 2x interpolation, no anti-image filter.

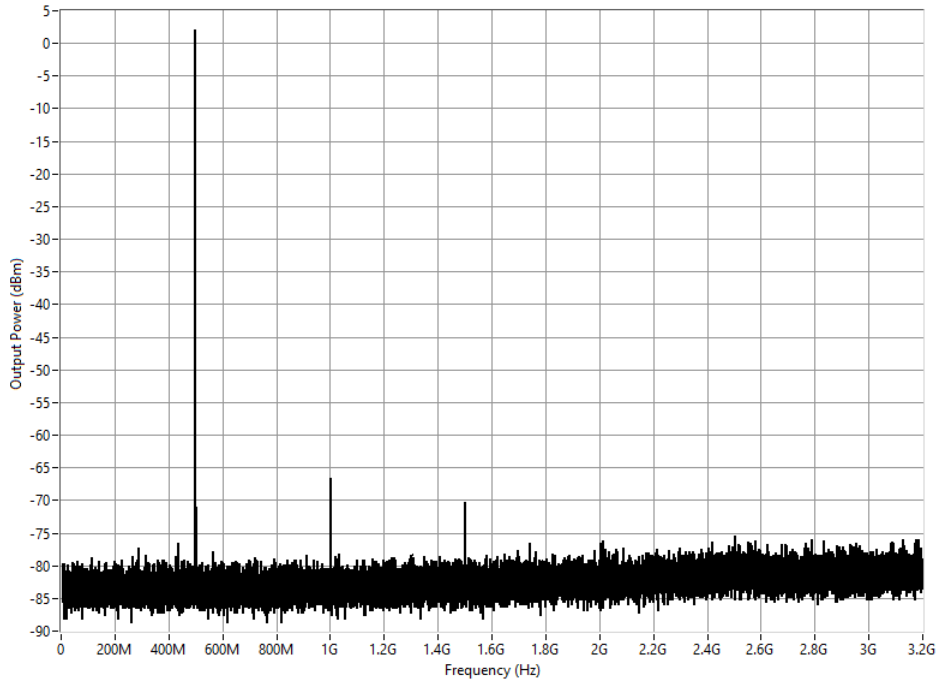
Table 10. IMD3 Performance, Dual Channel Mode, Measured[15]

	Generation Frequency	
	501 MHz and 511 MHz	**1.005 GHz and 1.015 GHz**
IMD3 (dBc)	-73.9	-67.6

Table 11. Noise Spectral Density[16]

	501 MHz Generation Frequency		
Mode	$\frac{nV}{\sqrt{Hz}}$	$\frac{dBm}{Hz}$	$\frac{dBFS}{Hz}$
Dual Channel	1.18	-165.5	-168.4
Single Channel	0.941	-167.5	-164.2

Figure 8. Single Tone Spectrum (Dual Channel Mode, 501 MHz 0 dBFS), Measured[17]



15. 2x interpolation, inverse sinc filter enabled, each tone corrected to -6 dBFS by inverse sinc filter.
16. Measured > 50 MHz offset from fundamental. 2x interpolation and inverse sinc filter enabled. Noise spectral density value depends on output tone frequency. See DAC38RF82 datasheet for noise spectral density results at other tone frequencies.
17. 2x interpolation. Output corrected to 0 dBFS by inverse sinc filter. 10 kHz resolution bandwidth.

Figure 9. Single Tone Spectrum (Dual Channel Mode, 1.01 GHz 0 dBFS), Measured[]

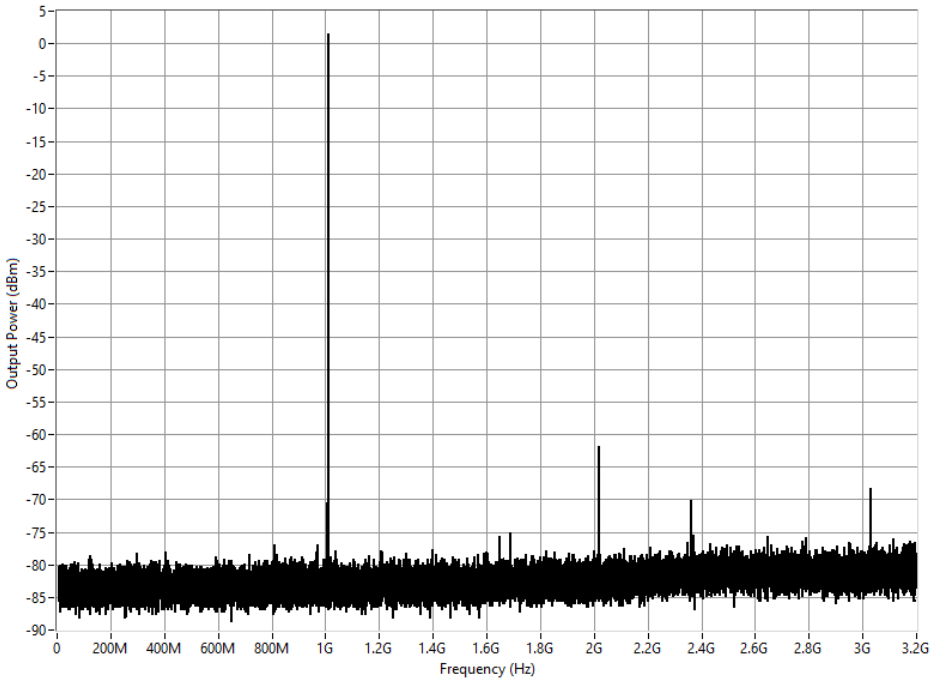
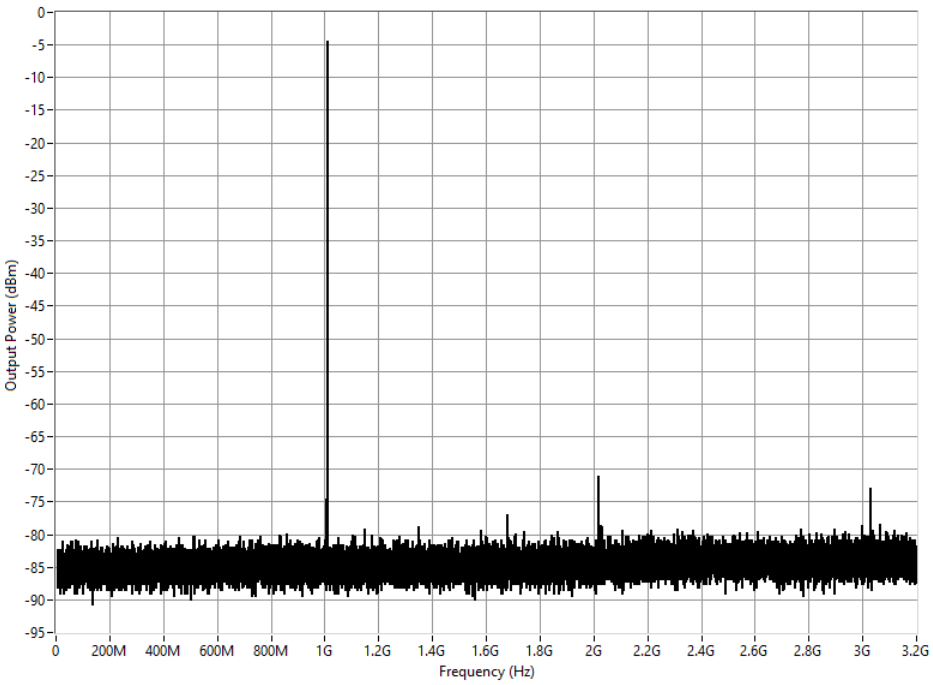


Figure 10. Single Tone Spectrum (Single Channel Mode, 1.01 GHz 0 dBFS), Measured[]

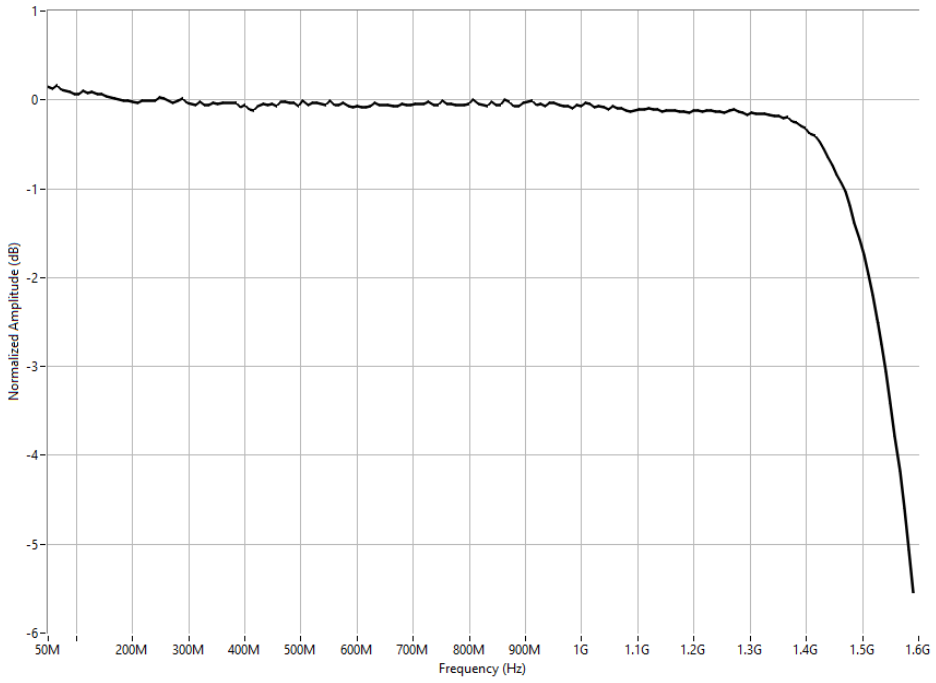


Channel-to-channel crosstalk, measured[18]	
100 MHz	-82 dBc

18. Aggressor channel generating a full-scale output into a 50 ohm terminator

500 MHz	-91 dBc
1.0 GHz	-90 dBc
1.5 GHz	-88 dBc
2.0 GHz	-82 dBc
2.5 GHz	-82 dBc

Figure 11. Analog Output Dual Channel Mode Frequency Response, Measured[19]



19. -6 dBFS, 2x Interpolation, inverse sinc filter enabled, no anti-image filter, normalized to 200 MHz.

Figure 12. Analog Output Single Channel Mode Frequency Response, No Anti-Image Filter, Measured

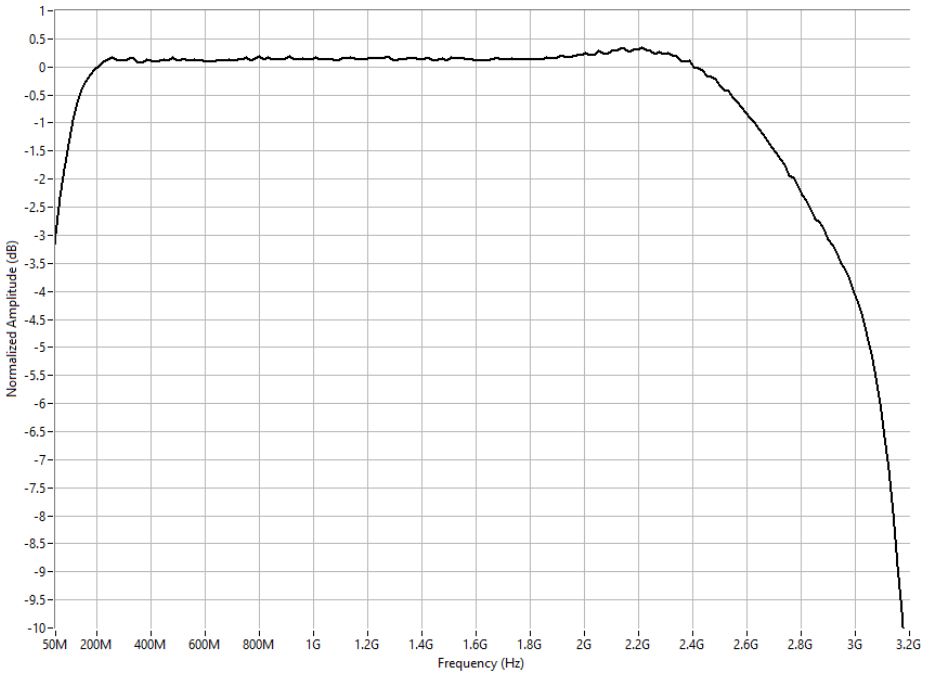
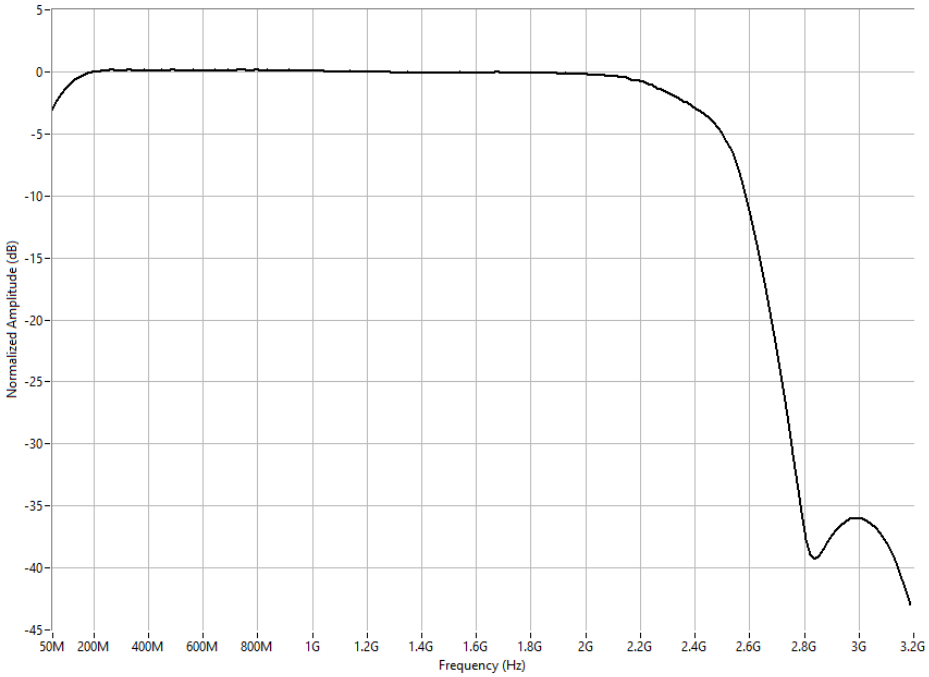
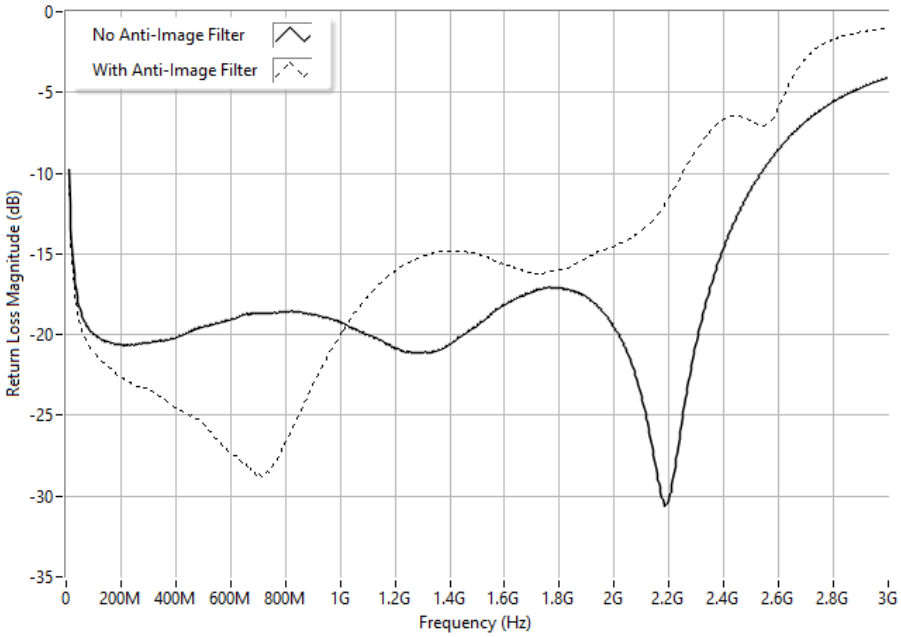


Figure 13. Analog Output Single Channel Mode Frequency Response With Anti-Image Filter, Measured[20]



20. -6 dBFS, 2x Interpolation, inverse sinc filter enabled, normalized to 200 MHz.

Figure 14. Analog Output Return Loss, Measured



REF/CLK IN

CLK/REF IN

Connector type	SMA
Input impedance	50 Ω
Input coupling	AC
Input voltage range	0.35 V pk-pk to 3.5 V pk-pk, nominal
Absolute maximum voltage	±12 V DC, 4 V pk-pk AC
Duty cycle	45% to 55%

Sample Clock jitter	
Analog input	86.8 fs_{rms}, measured[21]
Analog output	198.8 fs_{rms}, measured[22]

Table 12. Clock Configuration Options

Clock Configuration	External Clock Frequency	Description
Internal PXI_CLK10[23]	10 MHz	The internal Sample Clock locks to the PXI 10 MHz Reference Clock, which is provided through the backplane.
External Reference Clock (CLK/REF IN)	10 MHz [24]	The internal Sample Clock locks to an external Reference Clock, which is provided through the CLK/REF IN front panel connector.
External Sample Clock (CLK/REF IN)	2.8 GHz to 3.2 GHz	An external Sample Clock can be provided through the CLK/REF IN front panel connector.

21. Integrated from 3.2 kHz to 20 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.
22. Integrated from 1 kHz to 30 MHz. Includes the effects of the converter aperture uncertainty, converter PLL circuitry, and the clock circuitry jitter. Excludes trigger jitter.
23. Default clock configuration.
24. The external Reference Clock must be accurate to ±25 ppm.

Figure 15. Analog Input Phase Noise with 800 MHz Input Tone, Measured

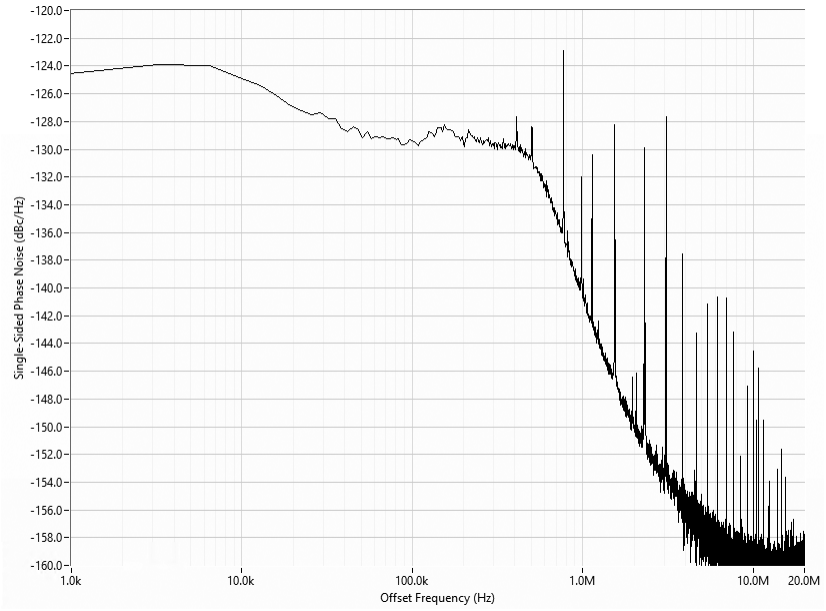
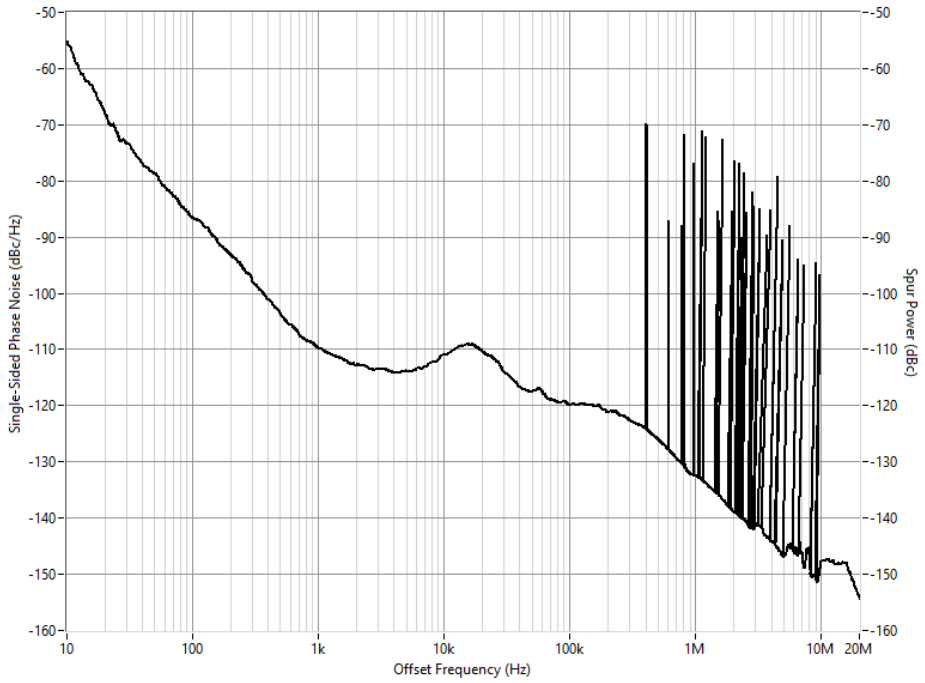


Figure 16. Analog Output Phase Noise with 1 GHz Output Tone, Measured



Bus Interface

Form factor	x8 PXI Express, specification v2.1 compliant

Maximum Power Requirements

Note Power requirements depend on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	3 A
+12 V	4 A
Maximum total power	58 W

Physical

Dimensions (not including connectors)	18.8 cm × 12.9 cm (7.4 in. × 5.1 in.)
Weight	190 g (6.7 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C[25] (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 4 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms}

25. The PXIe-5785 requires a chassis with slot cooling capacity ≥58 W. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to the PXI Chassis Manual for specifications to determine the ambient temperature ranges your chassis can achieve.

NI-TClk

You can use the NI-TClk synchronization method and the NI-TClk driver to align the Sample Clocks on any number of supported devices in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help* within the *FlexRIO Help*. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

Intermodule Synchronization Using NI-TClk for Identical Modules

Synchronization specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample Clocks of each module.
- All parameters are set to identical values for each module.
- Modules are synchronized without using an external Sample Clock.

Note Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

Skew[26]	80 ps, measured
Skew after manual adjustment	≤10 ps, measured
Sample Clock delay/adjustment	0.4 ps

26. Caused by clock and analog delay differences. No manual adjustment performed. Tested with a PXIe-1085 chassis with a 24 GB backplane with a maximum slot to slot skew of 100 ps. Measured at 23 °C.