PXIe-5413 Specifications

2025-04-11

Contents

PXIe-5413 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured* specifications describe the measured performance of a representative model.

Specifications are *Nominal* unless otherwise noted.

Conditions

All specifications are valid under the following conditions unless otherwise noted:

- Signals terminated with 50 Ω to ground
- Load impedance set to 50 Ω
- Amplitude set to 2.4 $V_{pk\text{-}pk}$
- Analog Path property or NIFGEN_ATTR_ANALOG_PATH attribute set to **Main** (default)
- Reference Clock set to **Onboard Reference Clock**

Warranted and typical specifications are valid under the following conditions unless otherwise noted:

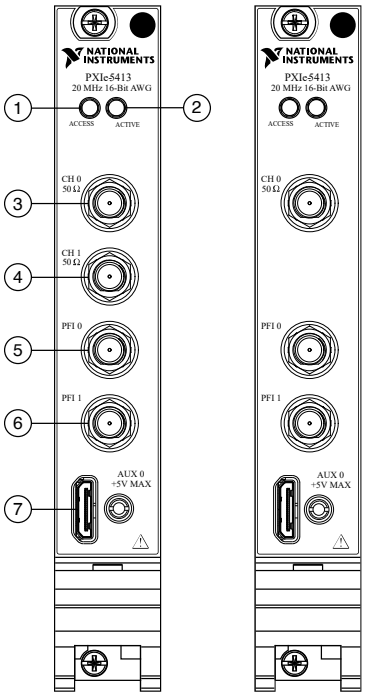
- Ambient temperature range of 0 °C to 55 °C
- 15-minute warm-up time before operation

- Self-calibration performed after instrument is stable
- External calibration cycle maintained and valid
- PXI Express chassis fan speed set to HIGH, foam fan filters removed if present, and empty slots contain PXI chassis slot blockers and filler panels

PXIe-5413 Pinout

The following figure shows the terminals on the PXIe-5413 connector.

Figure 1. PXIe-5413 Front Panel



1. Access LED
2. Active LED
3. SMA Connector: CH 0
4. SMA Connector: CH 1
5. SMA Connector: PFI 0
6. SMA Connector: PFI 1
7. MHDMR Connector: AUX 0

Table 1. SMA Connector Signal Descriptions

Signal	Access	Description
CH 0	Output	Generates waveforms from an analog output terminal.
CH 1		
PFI 0	Input/ Output	Imports digital trigger signals and exports digital event signals. • Imported digital trigger signals can start or step through waveform generation. • Exported event signals indicate the state of the generation engine.
PFI 1		

AUX 0 Connector Pinout

AUX 0, the MHDMR port on the PXIe-5413 front panel, routes digital trigger and event signals with eight bidirectional PFI lines and provides a +3.3 V power source.

AUX 0 also provides +24 V power for supported accessories.

Notice The AUX 0 connector accepts a standard, third-party HDMI™ type C cable, but the AUX 0 port is not an HDMI interface and the specified performance of the AUX 0 connector is not guaranteed if a third-party HDMI cable is used. Use NI cable assembly SHH19-MH19-AUX for all AUX 0 connections. Do not connect the AUX 0 port on the PXIe-5413 to the HDMI port of another instrument. NI is not liable for any damage resulting from such signal connections.

Figure 2. AUX 0 Connector Pinout

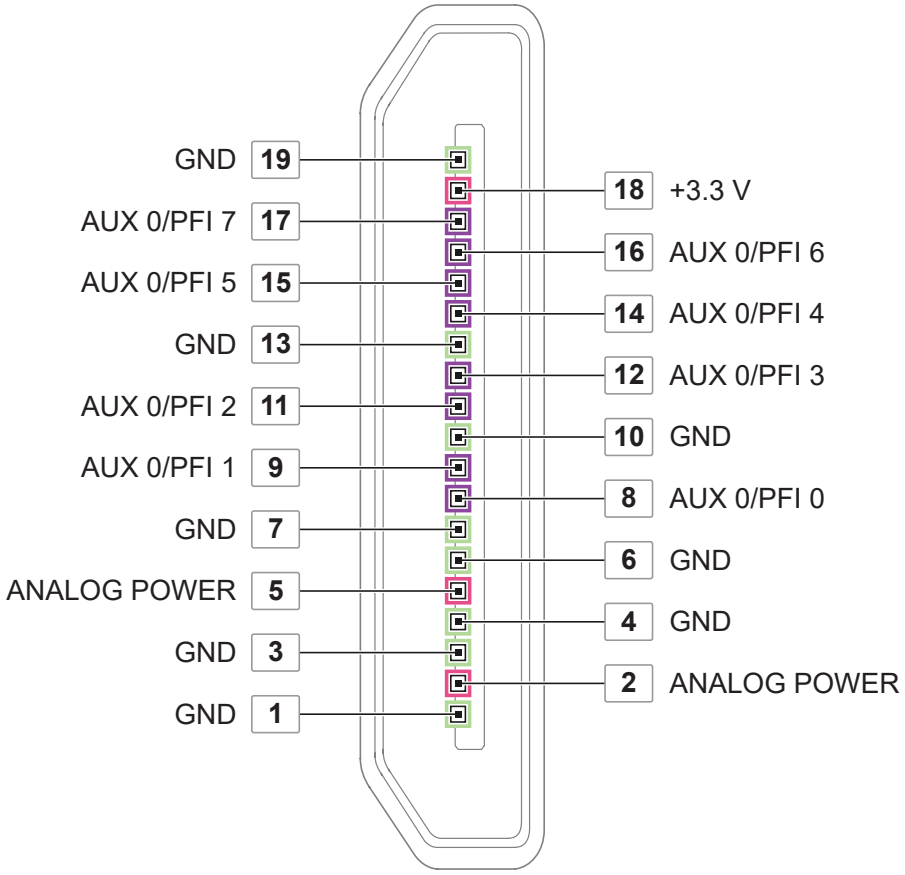


Table 2. Signal Descriptions

Signal Name	Description
GND	Ground reference for signals
ANALOG POWER[1]	Power output to supported connected accessories
AUX 0/PFI <0..7>	Bidirectional PFI line
+3.3 V	+3.3 V power output (200 mA maximum)

SCB-19 Pinout

NI recommends using the SCB-19 connector block to connect digital signals to the AUX 0 connector on the PXIe-5413 front panel.

1. Present starting with PXIe-5413 hardware revision (). NC (no connection) for prior revisions.

Figure 3. SCB-19 Pinout

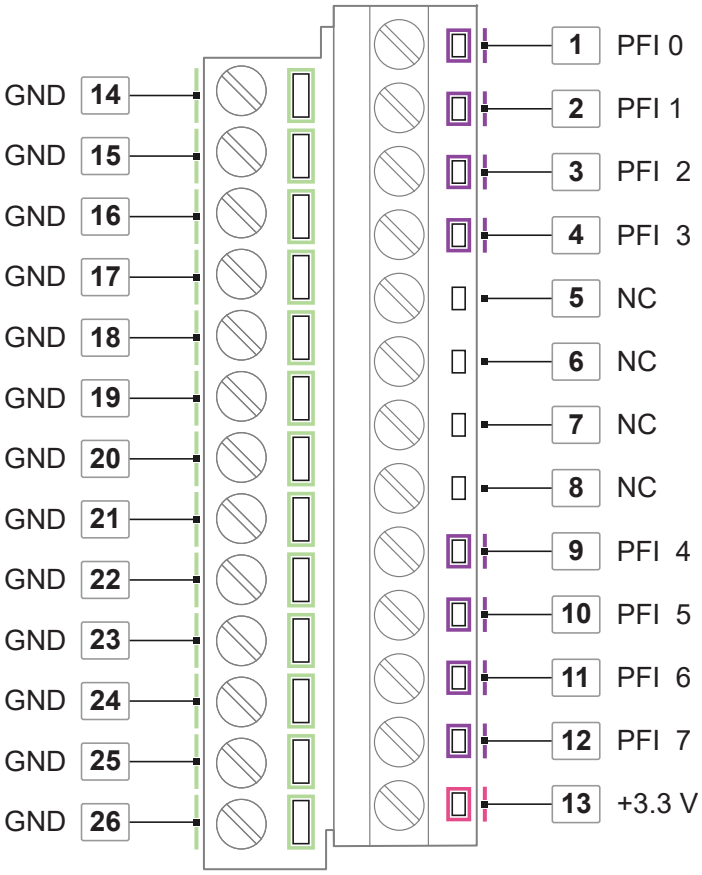


Table 3. SCB-19 Signal Descriptions

Signal Name	Description
PFI <0..7>	Bidirectional PFI line
NC	No connection
+3.3 V	+3.3 V power (200 mA maximum)
GND	Ground reference for signals

PXIe-5413 LED Indicators

The PXIe-5413 features an Access LED and Active LED.

Access LED

The Access LED, located on the module front panel, indicates module power and access.

The following table lists the Access LED states.

Table 4. ACCESS LED Indicator Status

Status Indicator	Indication
No color (off)	The module is not powered.
Amber	The module is being accessed.
Green	The module is powered and ready to be programmed.

Why Is the Access LED Off When the Chassis Is On?

The LEDs may not light until the module has been configured in Hardware Configuration Utility or MAX. Before proceeding, verify that the PXIe-5413 appears in Hardware Configuration Utility or MAX.

If the module appears in Hardware Configuration Utility or MAX but the Access LED fails to light after you power on the chassis, a problem may exist with the chassis power rails, a hardware module, or the LED.

Notice Apply external signals only when the PXIe-5413 is powered on. Applying external signals while the module is powered off may cause damage.

1. Disconnect any signals from the module front panel.
2. Power off the chassis.
3. Remove the module from the chassis and inspect it for damage.

   Notice Do not reinstall a damaged module.

4. Install the module in a different, supported slot within the same PXI chassis.
5. Power on the chassis.

   Note If you are using a PC with a module for PXI remote control system, power on the chassis before powering on the computer.

6. Verify that the module appears in Hardware Configuration Utility or MAX.
7. Call the niFgen Reset Device VI or niFgen_ResetDevice function to reset the module

and perform a self-test.
You can also perform a self-test in Hardware Configuration Utility or MAX.

Active LED

The Active LED, located on the module front panel, indicates the module output channel state.

The following table lists the Active LED states.

Table 5. Active LED Indicator Status

Status Indicator	Indication
(Off)	The module is not generating waveforms.
Amber	The module is armed and waiting for a trigger.
Green	The module has received a trigger and is generating a waveform.
Red	The module has detected an error.

Why Is the Active LED Red?

The red Active LED indicates that the instrument is in error state. The instrument will not operate until the error is cleared and/or the module is reset.

Note NI-FGEN must access the PXIe-5413 to determine the cause of the error.

Possible Error	Solution
The instrument has detected an unlocked condition on a PLL that might result in incorrect data. **Note** A PLL that is unlocked while in reset does not show an error.	To clear this error, call the niFgen Reset Device VI or niFgen_ResetDevice function to reset the instrument.
The instrument has been disabled because it exceeded its overall power limit.	
The instrument has been disabled because it	To re-enable the instrument, cool the instrument

Possible Error	Solution
exceeded its overall temperature limit.	to an acceptable range and resolve the environmental condition that caused the shutdown. To reset the instrument, call the niFgen Reset Device VI or niFgen_ResetDevice function, or power cycle the instrument.

Analog Output

Number of channels[2]	1 or 2
Output type	Referenced single-ended
Connector type	SMA
DAC resolution	16 bits

Amplitude range[3], in 0.16 dB steps	
50 Ω load	0.00775 V_{pk-pk} to 12 V_{pk-pk}
Open load	0.0155 V_{pk-pk} to 24 V_{pk-pk}

Offset range	±50% of *Amplitude Range* (V_{pk-pk})[4]

2. Channels support independent waveform generation.
3. Amplitude values assume the full scale of the DAC is utilized. NI-FGEN uses waveforms less than the full scale of the DAC to create amplitudes smaller than the minimum value.
4. For example, a 5.5 V_{pk-pk} range equals ±2.75 V maximum offset. Offset range has a limitation of ±12 V absolute signal swing into high-impedance loads ($Amplitude + |Offset| \leq 12$ V into high-impedance

Offset resolution	16-bit full-scale range

DC accuracy[5]	
Within ±5 °C of self-calibration temperature	±0.35% of *Amplitude Range* ± 0.35% of *Offset Requested* ± 500 µV, warranted[6]
0 °C to 55 °C	±0.55% of *Amplitude Range* ± 0.55% of *Offset Requested* ± 500 µV, typical

AC amplitude accuracy[7] (within ±5 °C of self-calibration temperature)	±1.0% ± 1 mV_{pk-pk}, warranted
Output impedance	50 Ω
Load impedance	Output waveform is compensated for user-specified impedances
Output coupling (ground referenced)	DC
Output enable[8]	Software-selectable

load or 6 V into 50 Ω load).

5. Terminated with high-impedance load (load impedance set to 1 MΩ). The analog path is calibrated for amplitude, gain, and offset errors.
6. Where *Amplitude Range* is the requested amplitude in V_{pk-pk}. For example, a DC signal with an amplitude range of 16 V_{pk-pk} and offset of 1.5 will calculate DC accuracy using the following equation: ±[(0.35% * 16 V) + (0.35% * 1.5 V) + 500 µV] = ±61.75 mV. The DC standard function always uses the 24 V_{pk-pk} amplitude range.
7. With 50 kHz sine wave and terminated with high-impedance load.

Maximum output overload[9]	±12 V_{pk-pk} from a 50 Ω source
Waveform summing	Supported[10]

Standard Function

Sine Waveform

Frequency range	0 MHz to 20 MHz
Frequency step size	2.84 µHz

Table 6. Passband Flatness[11]

Sine Frequency	**Passband Flatness (dB), Warranted**	
	0.06 V_{pk-pk} to 2.75 V_{pk-pk}	**>2.75 V_{pk-pk}**
1 MHz	±0.4	±0.4
10 MHz	±0.4	±0.4
20 MHz	±0.4	±0.6

8. When the output path is disabled, the channel output is terminated to ground with a 50 Ω, 1 W resistor.
9. No damage occurs if the analog output channels are shorted to ground indefinitely.
10. The output terminals of multiple PXIe-5413 waveform generators can be connected together.
11. Normalized to 50 kHz.

Figure 4. Passband Flatness

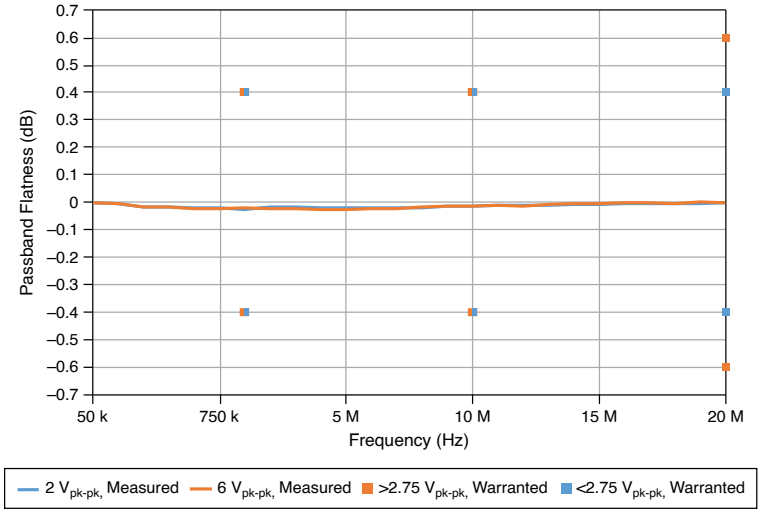


Table 7. Spurious-Free Dynamic Range (SFDR) with Harmonics

Sine Frequency	SFDR with Harmonics (dBc), Measured		
	0.1 V_{pk-pk} to 1 V_{pk-pk}	1 V_{pk-pk} to 2.75 V_{pk-pk}	>2.75 V_{pk-pk}
1 MHz	62	76	77
3 MHz	62	74	63
5 MHz	61	74	58
10 MHz	61	69	52
20 MHz	61	63	44

Note Measured at an amplitude of -1 dBFS with 0 V DC offset, measured from DC to 400 MHz, and limited to a -90 dBm spur at low amplitudes.

Table 8. Spurious-Free Dynamic Range (SFDR) without Harmonics

Sine Frequency	SFDR without Harmonics (dBc), Measured		
	0.1 V_{pk-pk} to 1 V_{pk-pk}	1 V_{pk-pk} to 2.75 V_{pk-pk}	>2.75 V_{pk-pk}
1 MHz	62	84	92
3 MHz	62	84	92
5 MHz	62	84	92

Sine Frequency	SFDR without Harmonics (dBc), Measured		
	0.1 V_{pk-pk} to 1 V_{pk-pk}	1 V_{pk-pk} to 2.75 V_{pk-pk}	>2.75 V_{pk-pk}
10 MHz	61	83	90
20 MHz	61	83	90

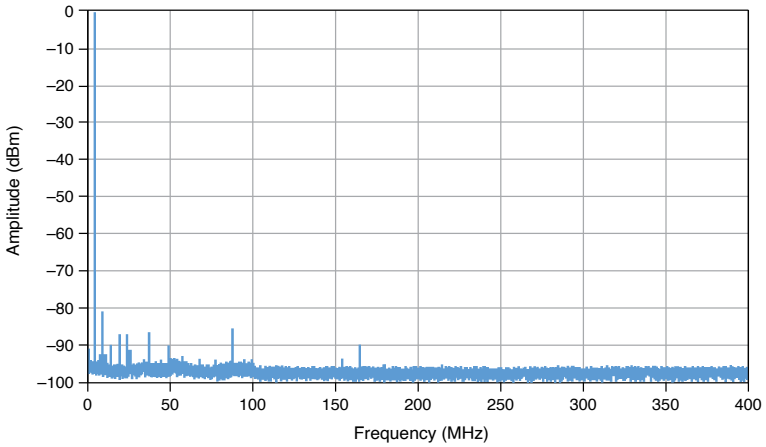
Note Measured at an amplitude of -1 dBFS with 0 V DC offset, measured from DC to 400 MHz, and limited to a -90 dBm spur at low amplitudes.

Table 9. Total Harmonic Distortion (THD)

Sine Frequency	THD (dBc), Measured	
	0.1 V_{pk-pk} to 2.75 V_{pk-pk}	2.75 V_{pk-pk} to 12 V_{pk-pk}
1 MHz	79	76
3 MHz	73	62
5 MHz	72	56
10 MHz	68	49
20 MHz	61	43

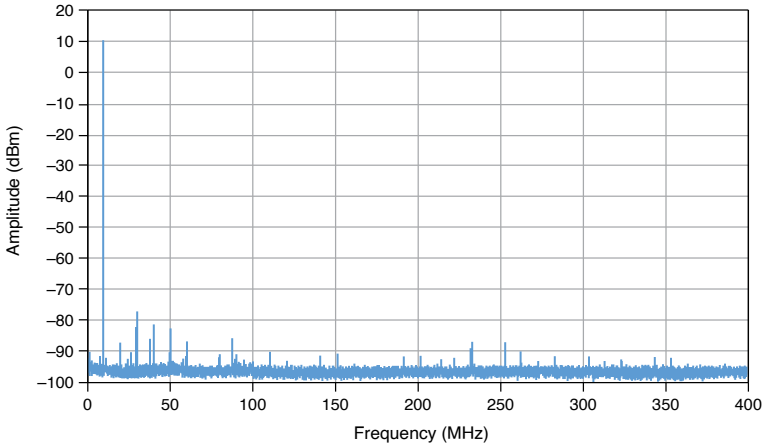
Note Measured at an amplitude of -1 dBFS and measured from DC to the sixth harmonic.

Figure 5. 5 MHz Spectrum at 0.6 V_{pk-pk}, Measured



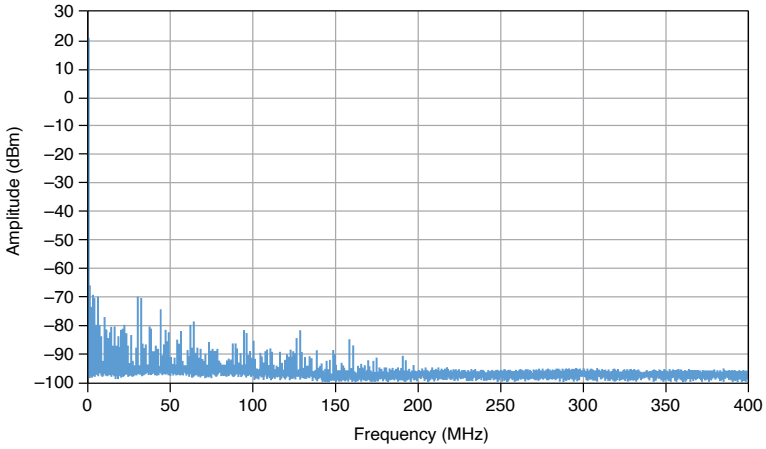
Note Noise floor is limited by the noise floor of the measurement device.

Figure 6. 10 MHz Spectrum at 2 V_{pk-pk}, Measured



Note Noise floor is limited by the noise floor of the measurement device.

Figure 7. 1 MHz Spectrum at 6.5 V_{pk-pk}, Measured



Note Noise floor is limited by the noise floor of the measurement device.

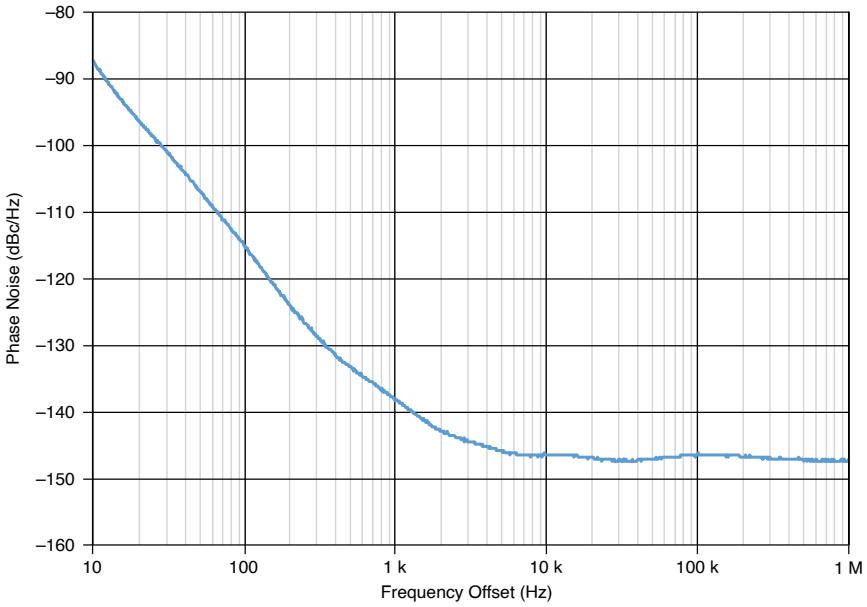
Table 10. Average Noise Density[12]

Amplitude	Average Noise Density, Typical	
	dBm/Hz	$\frac{nV}{\sqrt{Hz}}$
0.06 V_{pk-pk}	-154	3.9
0.1 V_{pk-pk}	-154	3.9

12. At small amplitudes, average noise density is limited by a -154 dBm/Hz noise floor.

Amplitude	Average Noise Density, Typical	
	dBm/Hz	$\frac{nV}{\sqrt{Hz}}$
0.4 V_{pk-pk}	-150	5.8
1 V_{pk-pk}	-145	13
2 V_{pk-pk}	-141	20
4 V_{pk-pk}	-132	53
12 V_{pk-pk}	-125	107

Figure 8. Phase Noise[13], Measured



Jitter (RMS)[14]	239 fs

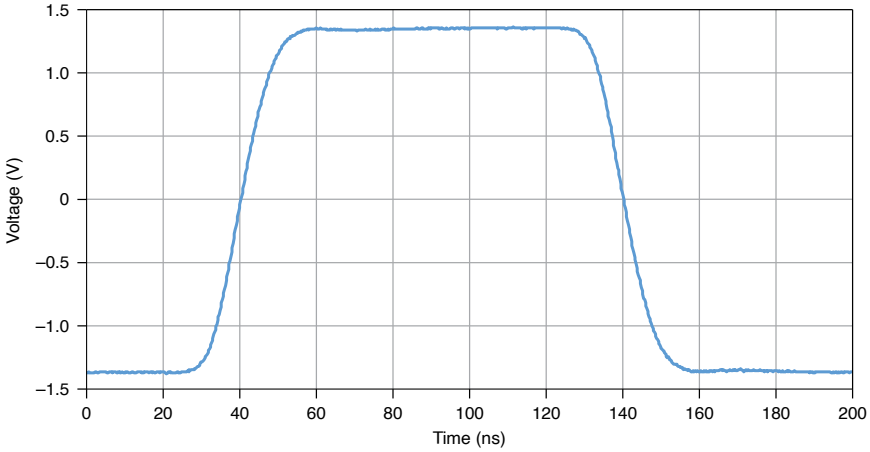
Square Waveform

Frequency range	0 MHz to 10 MHz

13. With 20 MHz carrier and locked to the internal timebase with spurs removed.
14. With 20 MHz carrier, integrated from 100 Hz to 100 kHz, and locked to the internal timebase.

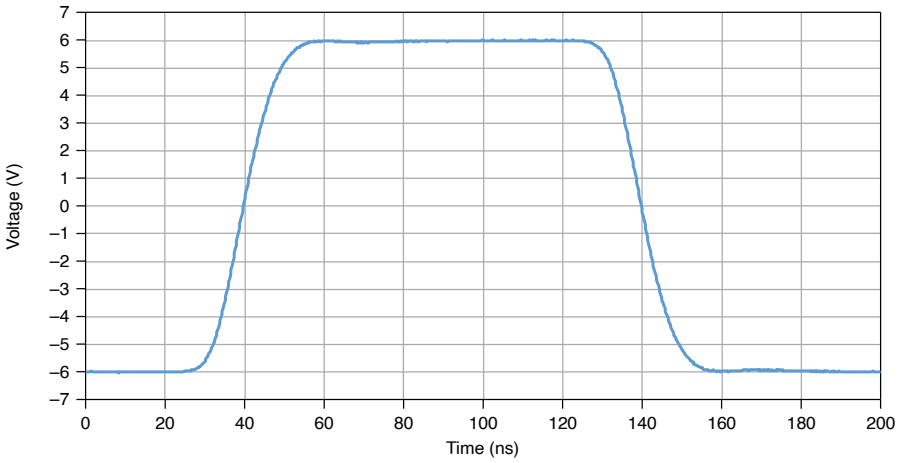
Frequency step size	2.84 µHz
Minimum on/off time[15]	38.5 ns
Duty cycle resolution	<0.001%
Rise/fall time[16]	17 ns, measured
Aberration	1.0%, measured
Jitter (RMS)[17]	5 ps, measured

Figure 9. Square Waveform Step Response at 2.75 V_{pk-pk}, Measured



15. Used for calculating duty cycle limit:
Minimum Duty Cycle = (100% * *Minimum On Time*) ÷ T_{period}
and *Maximum Duty Cycle* = 100% - *Minimum Duty Cycle*. For more information about the relationship between minimum on/off time and duty cycle specifications, refer to ni.com.
16. Rise time measured from 10% to 90%.
17. Integrated from 10 Hz to 4 MHz using a 10 MHz square wave.

Figure 10. Square Waveform Step Response at 12 V_{pk-pk}, Measured



Ramp and Triangle Waveforms

Frequency range	0 MHz to 1 MHz

User-Defined Function

Frequency range	0 MHz to 20 MHz
Frequency step size	2.84 µHz
Waveform points	8,192
Step response rise time	14.8 ns, measured

Arbitrary Waveform

Waveform size	2 samples to 64,000,000 samples

User sample rate	
Digital filter enabled	5.6 µS/s to 200 MS/s
Digital filter disabled	3.125 MS/s to 200 MS/s

Waveform filters	
Digital filter enabled	*Bandwidth* = 0.2 * *User Sample Rate*
Digital filter disabled	No reconstruction image rejection

Minimum quantum size	1 sample

Rise time[18]	
Digital filter enabled	20.3 ns, measured
Digital filter disabled	16.3 ns, measured

Total onboard memory	128 MB per channel

18. At maximum user sample rate.

Figure 11. Magnitude Response[19], Measured

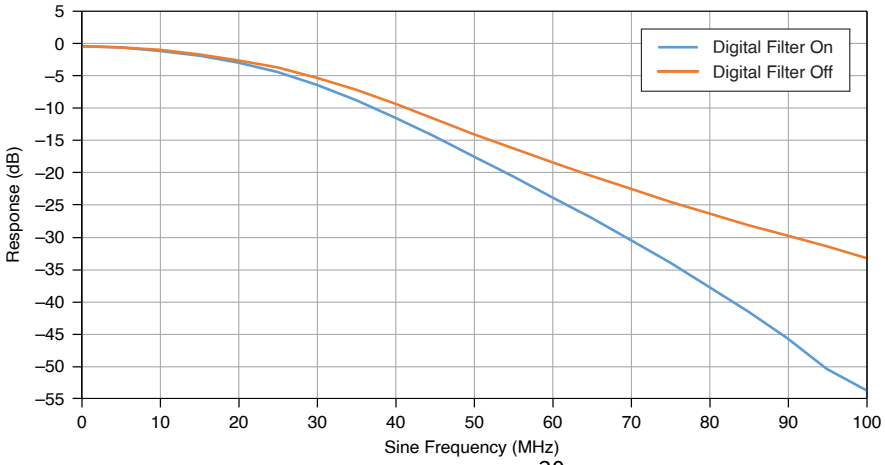


Figure 12. 10 MHz Single-Tone Spectrum[20], Measured

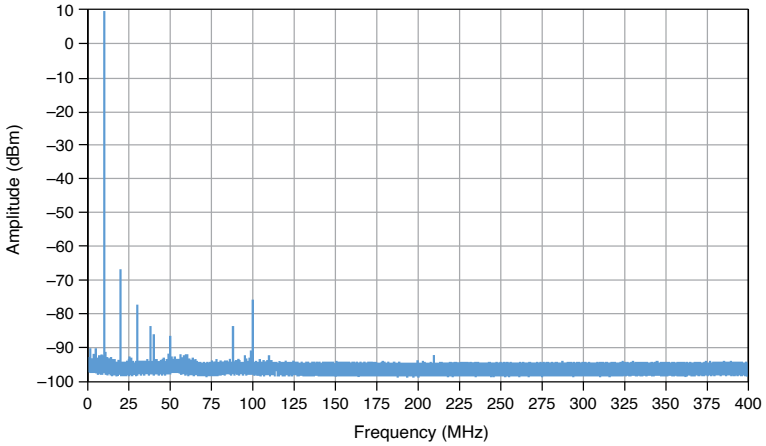
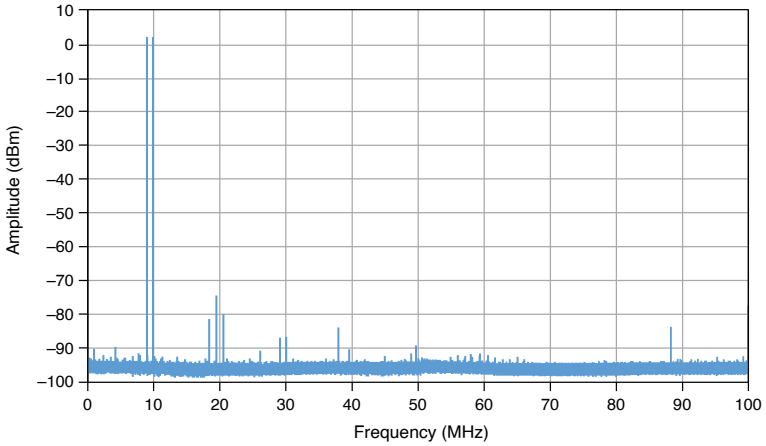


Figure 13. 9.5 MHz and 10.5 MHz Dual-Tone Spectrum[21], Measured



19. Relative to 50 kHz and at 2 V_{pk-pk} and maximum user sample rate.
20. With the digital filter enabled and at -1 dBFS, 2 V_{pk-pk}, and 200 MS/s. Noise floor is limited by the noise floor of the measurement device.
21. With the digital filter enabled and at -7 dBFS, 2 V_{pk-pk}, and 200 MS/s. Noise floor is limited by the noise floor of the measurement device.

All Output Modes

Figure 14. Channel-To-Channel Crosstalk, Measured

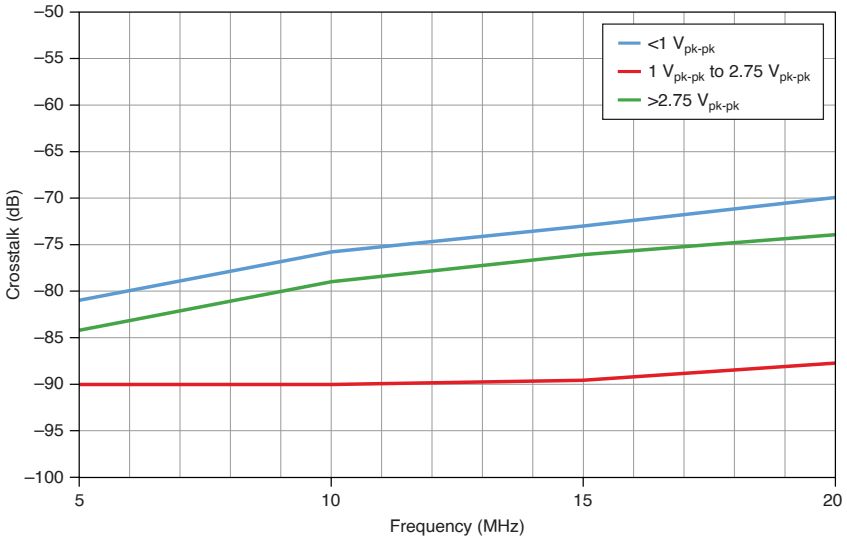
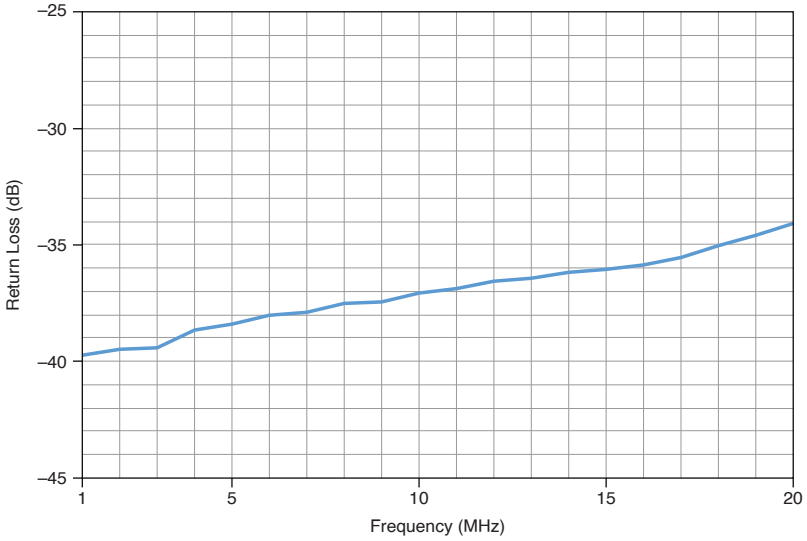


Figure 15. Return Loss, Measured



Clock

Reference Clock source	Internal PXIe_CLK100 (backplane connector)
Reference Clock frequency	100 MHz (<±25 ppm)

Sample Clock rate	800 MHz

Internal timebase accuracy[22]	
Initial calibrated accuracy	1.5 ppm, warranted
Time drift[23]	1 ppm per year, warranted
Accuracy	*Initial Calibrated Accuracy* ± *Time Drift*, warranted

Synchronization

Channel-to-channel skew, between the channels of a multichannel PXIe-5413 [24]	
<2.75 Vpk-pk	±110 ps
>2.75 Vpk-pk	±275 ps

Note The channels of a multichannel PXIe-5413 are automatically synchronized when they are in the same NI-FGEN session.

Synchronization with the NI-TClk API

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PXIe-5413 and NI-FGEN.

22. If locked to an external Reference Clock source, timebase accuracy is equal to the external Reference Clock accuracy.
23. Where time drift starts at the latest external calibration date.
24. With a 20 MHz sine wave and both channels configured with the same amplitude.

NI-TClk synchronization support for the PXIe-5413 was first available in NI-FGEN18.1.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

The following definitions apply:

- **Skew**—Misalignment between module timing across slots of a chassis and is caused by clock and analog path delay differences.
- **Jitter**—Variation in module alignment that can be expected with each call to NI-TClk Synchronize.
- **Manual adjustment**—Process of minimizing synchronization jitter and skew by adjusting Trigger Clock (TClk) signals using the instrument driver.

Module-to-module skew, between PXIe-5413 modules using NI-TClk [25]	
NI-TClk synchronization without manual adjustment	
Skew, peak-to-peak	300 ps, typical
Jitter, peak-to-peak	125 ps, typical
NI-TClk synchronization with manual adjustment	
Skew, average	<10 ps
Jitter, peak-to-peak	5 ps

25. Specifications are valid for any number of PXIe-5413 modules installed in one chassis, with each PXIe-5413 module using a single NI-FGEN session and having all analog parameters set to identical values, and Sample Clock set to 100 MS/s. For other configurations, including multi-chassis systems, contact NI Technical Support at ni.com/support.

Sample Clock delay/adjustment resolution	3.8E(-6) × *Sample Clock Period* For example, at 100 MS/s, 3.8E(-6) × (1/100 MS/s) = 38 fs.

PFI I/O

Number of terminals	10

Connector type	
PFI 0 and PFI 1	SMA
AUX 0/PFI <0..7>	MHDMR

Logic level	3.3 V
Maximum input voltage	+5 V
V_{IH}	2 V
V_{IL}	0.8 V
Frequency range	0 MHz to 25 MHz

PFI-to-channel crosstalk	-80 dBc, measured

Trigger

Sources/destinations	PFI <0..1> (SMA front panel connectors) AUX 0/PFI <0..7> (MHDMR front panel connector) PXI_Trig <0..7> (backplane connector)
Supported triggers	Start Trigger
Trigger type	Rising edge
Trigger modes[26]	Single Continuous Stepped Burst
Input impedance (DC)	>100 kΩ

Marker

Destinations	PFI <0..1> (SMA front panel connectors) AUX 0/PFI <0..7> (MHDMR front panel connector)

26. In frequency list, arbitrary waveform, and arbitrary sequence output modes.

	PXI_Trig <0..7> (backplane connector)
Pulse width	200 ns

Marker to output skew	
PFI <0..1> and AUX 0/PFI <0..7>	±2 ns
PXI_Trig <0..7>	±20 ns

Maximum number of marker outputs per waveform	4

Calibration

Self-calibration	An onboard reference is used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 2 minutes to complete.
External calibration	External calibration calibrates the TCXO, voltage reference, and DC gain and offset. Appropriate constants are stored in nonvolatile memory.
Calibration interval	Specifications valid within 2 years of external calibration
Warm-up time[27]	15 minutes

27. Warm up begins after the chassis is powered and the PXIe-5413 is recognized by the host and

Power

Current	
+3.3 V rail	2.3 A
+12 V rail	1.8 A
Total power	29 W

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C
Relative humidity range	10% to 90%, noncondensing

configured using NI-FGEN. Self-calibration is recommended following the warm-up time.

Storage Environment

Ambient temperature range	-40 °C to 71 °C
Relative humidity range	5% to 95%, noncondensing

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms}

Physical

Dimensions	21.6 cm × 2.0 cm × 13.0 cm (8.5 in. × 0.8 in. × 5.1 in.) 3 U, one slot, PXI Express module
Weight	
One channel	369 g (13.0 oz)
Two channels	376 g (13.3 oz)
Bus interface	

Form factor	Gen 1 x4 module
Slot compatibility	PXI Express or hybrid

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In

Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Engineering a Healthy Planet* web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)