PXIe-5162 Specifications

2026-03-18

Contents

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These specifications apply to the PXIe-5162.

Revision History

Version	Date changed	Description
373858L-01	March 2026	Removed 64 MB onboard memory variant.
373858K-01	January 2025	Added pinouts
373858G-01	March 2018	Renamed to PXIe-5162.
375320A-01	December 2012	Initial release.

Looking For Something Else?

For information not found in the specifications for your product, such as operating instructions, browse *Related Information*.

Related information:

- PXIe-5160/5162 Getting Started Guide
- PXIe-5162 Calibration Procedure
- Software and Driver Downloads
- PXIe-5162 Dimensional Drawings
- PXIe-5162 Product Certifications
- PXIe-5160/5162 Letter of Volatility
- Discussion Forums

Definitions

Warranted specifications describe the performance of a model under stated operating

conditions and are covered by the model warranty. *Warranted* specifications account for measurement uncertainties, temperature drift, and aging. *Warranted* specifications are ensured by design, or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured (meas)* specifications describe the measured performance of a representative model.

Specifications are *Typical* unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges
- All bandwidths and bandwidth limit filters
- Sample rate set to 1.25 GS/s, 2.5 GS/s, or 5 GS/s
- Onboard Sample clock locked to onboard Reference clock

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature ranges of 0 °C to 45 °C
- The PXIe-5162 is warmed up for 15 minutes at ambient temperature
- Self-calibration is completed after warm-up period
- Calibration cycle is maintained
- The PXI Express chassis fan speed is set to HIGH, the foam fan filters are removed if present, and the empty slots contain PXI chassis slot blockers and filler panels. For more information about cooling, refer to the Maintain Forced-Air Cooling Note to Users document available at ni.com/docs.
- NI-SCOPE 4.1 or later instrument driver is used
- External calibration is performed at 23 °C ± 3 °C

Typical specifications are valid under the following conditions unless otherwise noted:

- Ambient temperature ranges of 0 °C to 45 °C

PXIe-5162 Pinout

Use the pinout to connect to terminals on the PXIe-5162.

Figure 1. PXIe-5162 Connector Pinout

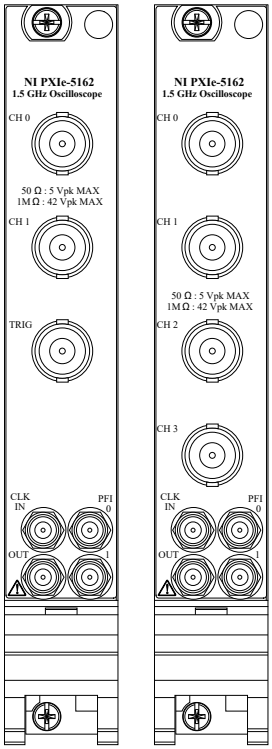


Table 1. PXIe-5162 (2CH) Front Panel Connectors

Label	Function	Connector Type
CH 0 and CH 1	Analog input connection; digitizes data and triggers acquisitions.	BNC female
TRIG	External analog trigger; signals on the TRIG connector cannot be digitized.	BNC female
CLK IN	Imports an external Reference Clock or Sample Clock to the device.	SMB jack

Label	Function	Connector Type
CLK OUT	Exports the Reference Clock from the device.	SMB jack
PFI 0	PFI line for digital trigger input/output.	SMB jack
PFI 1	PFI line for digital trigger input/output and probe compensation. No subsample trigger accuracy.	SMB jack

Table 2. PXIe-5162 (4CH) Front Panel Connectors

Label	Function	Connector Type
CH 0 to CH 3	Analog input connection; digitizes data and triggers acquisitions.	BNC female
CLK IN	Imports an external Reference Clock or Sample Clock to the device.	SMB jack
CLK OUT	Exports the Reference Clock from the device.	SMB jack
PFI 0	PFI line for digital trigger input/output.	SMB jack
PFI 1	PFI line for digital trigger input/output and probe compensation. No subsample trigger accuracy.	SMB jack

Vertical

Analog Input

Number of channels	
PXIe-5162 (2 CH)	Two (simultaneously sampled)

PXIe-5162 (4 CH)	Four (simultaneously sampled)
Input type	Referenced single-ended
Connectors	BNC

Impedance and Coupling

Note Impedance and coupling are software-selectable on a per-channel basis.

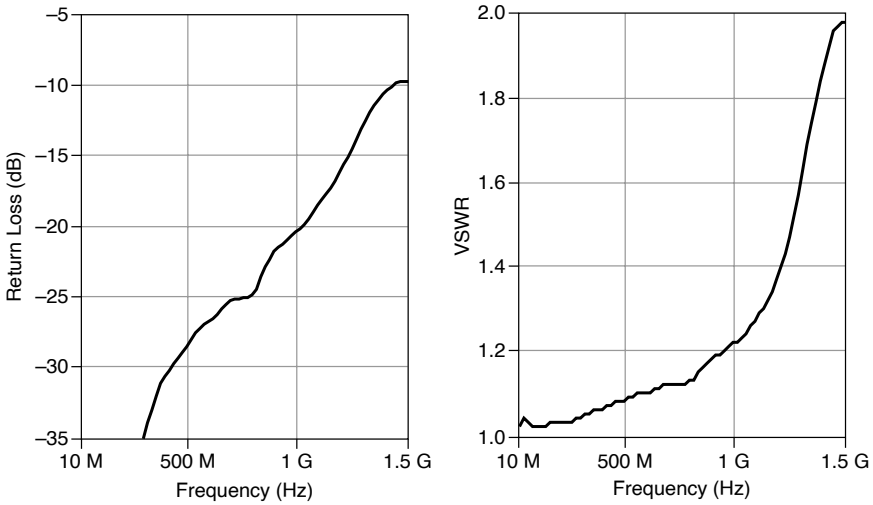
Table 3. Input Impedance

Impedance Setting	Typical	Warranted
50 Ω	50 Ω ± 1.50%	50 Ω ± 1.75%
1 MΩ	1 MΩ ± 0.75%	1 MΩ ± 0.90%

Input capacitance[1]	15 pF ± 0.8 pF, nominal 15 pF ± 2.5 pF, warranted
Input coupling	AC, DC

1. 1 MΩ input only.

Figure 2. 50 Ω Input Return Loss and Input VSWR, Measured



Voltage Levels

Table 4. 50 Ω Full-Scale (FS) Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	Vertical Offset Range (V)
0.05 V	±0.5
0.1 V	±0.5
0.2 V	±0.5
0.5 V	±0.5
1 V	±0.5
2 V	±1.5
5 V	0

Table 5. 1 MΩ FS Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	Vertical Offset Range (V)
0.05 V	±0.5
0.1 V	±0.5
0.2 V	±0.5
0.5 V	±0.5
1 V	±0.5
2 V	±5

Input Range (V_{pk-pk})	Vertical Offset Range (V)
5 V	±5
10 V	±5
20 V	±30
50 V	±15

Maximum input overload[2]	
50 Ω	|Peaks| ≤5 V, nominal
1 MΩ	|Peaks| ≤42 V, nominal

Accuracy

Resolution	10 bits
DC accuracy[3][3]	±[(2% × |*Reading* - *Vertical Offset*|) + (1.4% × |*Vertical Offset*|) + (0.6% of *FS*) + 600 µV]
DC drift[4][4]	±[(0.1% × |*Reading* - *Vertical Offset*|) + (0.025% × |*Vertical Offset*|) + (0.03% of *FS*)] per °C, nominal
AC amplitude accuracy[3]	±0.5 dB at 50 kHz

2. Signals exceeding the maximum input overload may cause damage to the device.
3. Within ±3 °C of self-calibration temperature. This specification is *typical* for peak-to-peak input ranges of 0.05 V to 0.1 V and *warranted* for all other input ranges.
4. Used to calculate errors when onboard temperature changes more than ±3 °C from the self-calibration temperature.

AC amplitude drift[4]	±0.01 dB per °C at 50 kHz, nominal

Table 6. Channel-to-Channel Crosstalk, Nominal[5]

Input Impedance	Input Frequency	Crosstalk
50 Ω [5]	DC ≤ *f* ≤ 100 MHz	-60 dB
	100 MHz < *f* ≤ 700 MHz	-45 dB
	700 MHz < *f* ≤ 1000 MHz	-40 dB
1 MΩ[6]	DC ≤ *f* ≤ 100 MHz	-55 dB
	100 MHz < *f* ≤ 200 MHz	-45 dB

Bandwidth and Transient Response

50 Ω bandwidth (-3 dB)[7]	1.5 GHz, warranted

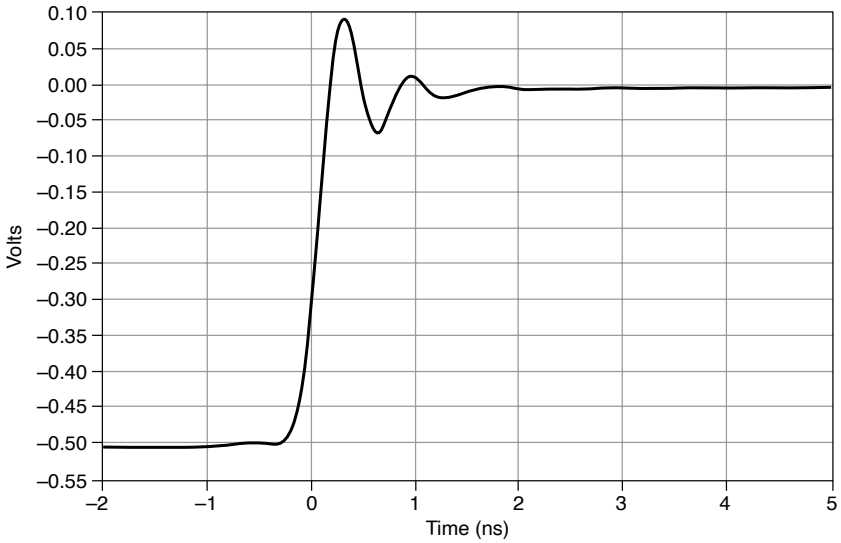
Table 7. 1 MΩ Bandwidth (-3 dB)[11]

Input Impedance	Input Range (V_{pk-pk})	Nominal	Warranted[8]
1 MΩ [9]	0.05 V to 1 V	—	300 MHz
	2 V to 10 V	300 MHz	250 MHz[10]
	20 V to 50 V	300 MHz	—

5. Measured on one channel with test signal applied to another channel with the same range setting on both channels.
6. Only valid on peak-to-peak input ranges of 0.05 V to 10 V.
7. Normalized to 50 kHz.
8. For ambient temperature ranges of 0 °C to 30 °C
9. Verified using a 50 Ω source and 50 Ω feed-through terminator.
10. For ambient temperature ranges of 0 °C to 30 °C

Bandwidth-limiting filters[11]	20 MHz 175 MHz
Rise/fall time[12]	
50 Ω	320 ps
1 MΩ[13]	1.4 ns
AC-coupling cutoff (-3 dB)[14]	
50 Ω[15]	170 kHz
1 MΩ	17 Hz

Figure 3. PXIe-5162 Step Response, 50 Ω, 1 V_{pk-pk} Input Range, -0.25 V Programmable Offset, 150 ps Rising Edge, Measured



11. Normalized to 50 kHz.
12. 50% FS input pulse.
13. Verified using a 50 Ω source and 50 Ω feed-through terminator.
14. Verified using a 50 Ω source.
15. With AC coupling enabled, the DC resistance to ground is 20 kΩ.

Figure 4. PXIe-5162 Step Response, 1 MΩ, 1 V_{pk-pk} Input Range, -0.25 V Programmable Offset, 500 ps Rising Edge, Measured [16]

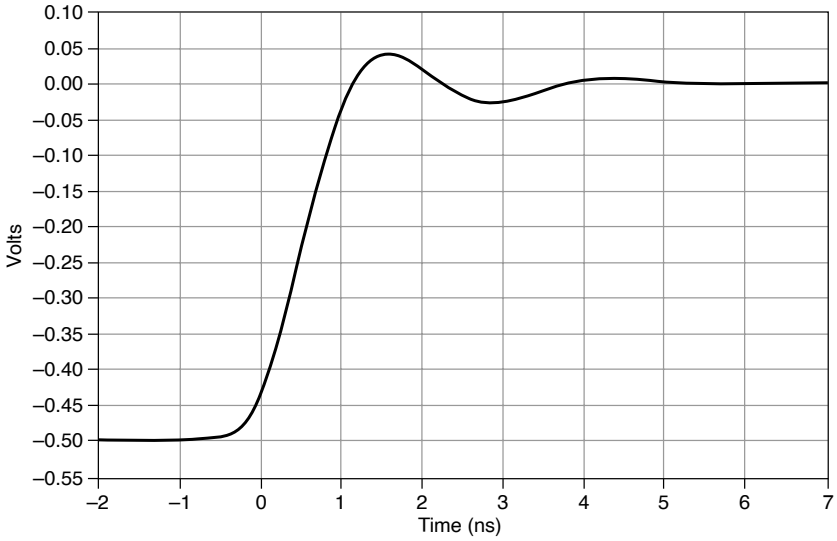
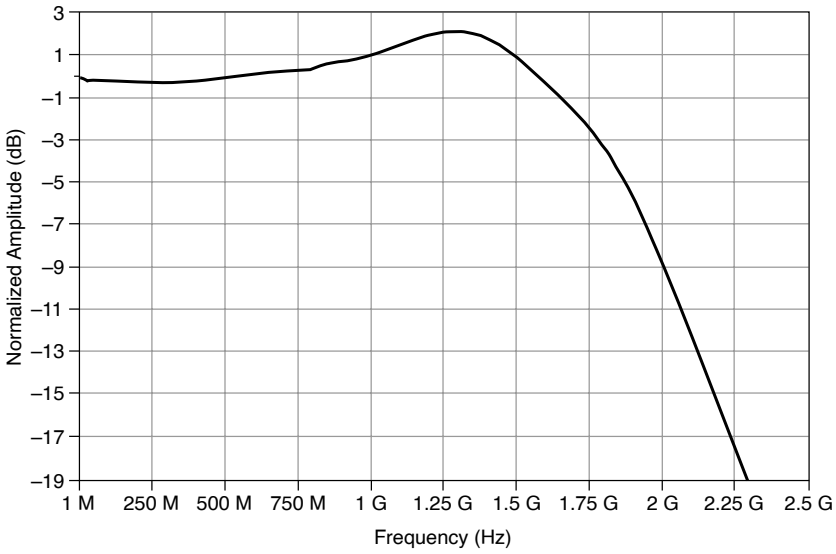


Figure 5. PXIe-5162 50 Ω Frequency Response, 1 V_{pk-pk}, 5 GS/s, Measured



16. Verified using a 50 Ω source and 50 Ω feed-through terminator.

Figure 6. PXIe-5162 1 MΩ Frequency Response, 1 V_{pk-pk}, Measured [17]

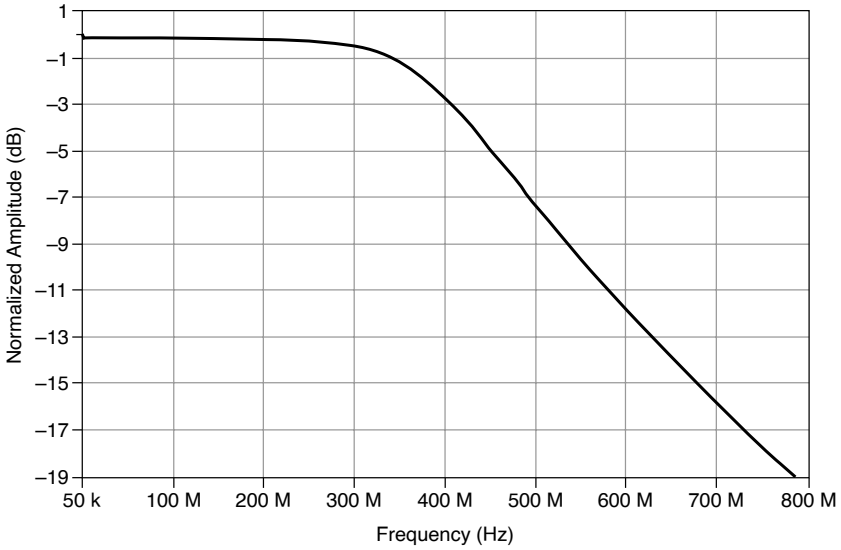
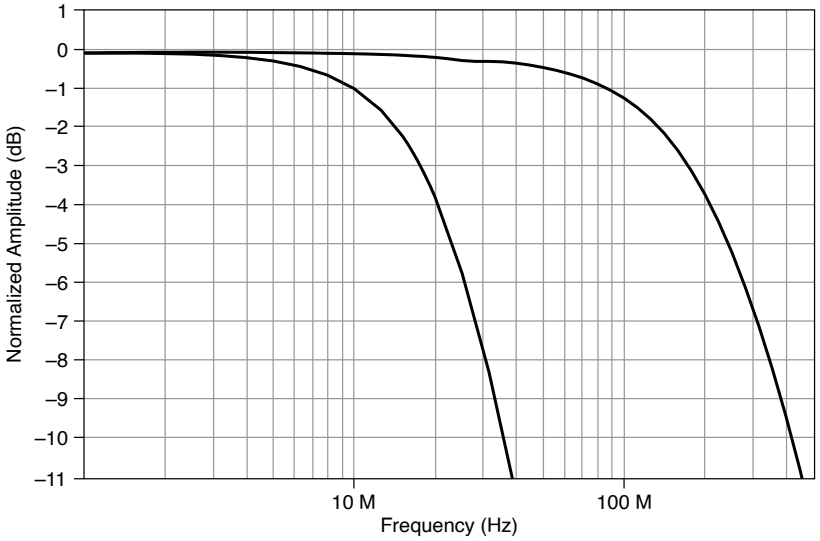


Figure 7. PXIe-5162 Bandwidth-Limiting Filters Frequency Response, 1 V_{pk-pk}, Measured



17. Verified using a 50 Ω source and 50 Ω feed-through terminator.

Spectral Characteristics

50 Ω Spectral Characteristics

Table 8. Spurious-Free Dynamic Range (SFDR), Measured[18]

Input Frequency	Input Range (V_{pk-pk})	SFDR	
		1.25 GS/s [18], 2.5 GS/s[19], 5.0 GS/s[19]	2.5 GS/s, 5.0 GS/s
<10 MHz	0.05 V	52 dBc	40 dBc
	0.1 V	52 dBc	46 dBc
	0.2 V	56 dBc	46 dBc
	0.5 V to 5 V	56 dBc	50 dBc
≥10 MHz to ≤1 GHz	0.05 V	46 dBc	40 dBc
	0.1 V to 5 V	46 dBc	46 dBc

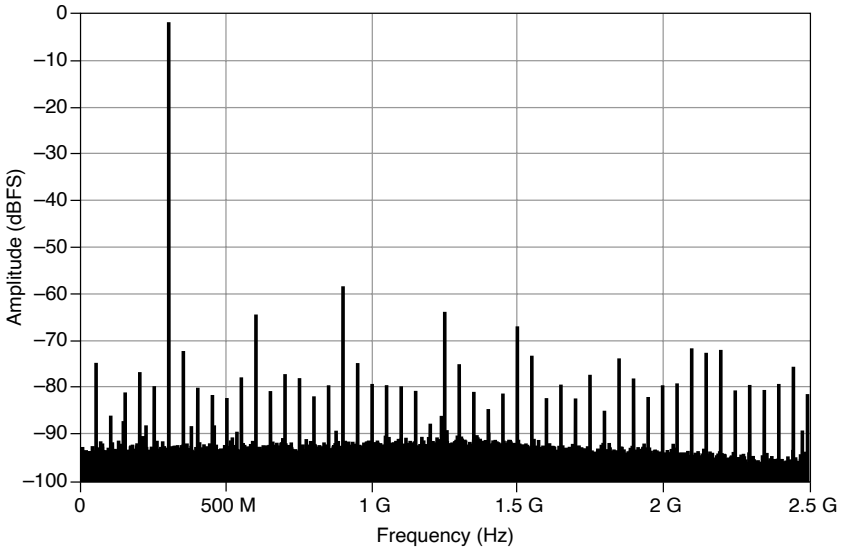
Table 9. Effective Number of Bits (ENOB), Nominal[18]

Input Frequency	Input Range (V_{pk-pk})	ENOB
<1 GHz	0.05 V	6.0
	0.1 V	6.6
	0.2 V to 5 V	7.0

Figure 8. PXIe-5162 Single-Tone Spectrum, 2.98 dBm Input Signal at Connector, 50 Ω, 1 V_{pk-pk}, 5 GS/s,

18. -1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics. 7.2 kHz resolution bandwidth.
19. Excludes ADC interleaving spurs.

300 MHz Input Tone, Full Bandwidth, Measured



1 MΩ Spectral Characteristics[20]

Table 10. SFDR, Nominal[21]

Input Frequency	Input Range (V_{pk-pk})	SFDR	
		1.25 GS/s[21], 2.5 GS/s[22][22], 5.0 GS/s[22]	2.5 GS/s, 5.0 GS/s
<10 MHz	0.05 V to 10 V	53 dBc	48 dBc
	20 V	50 dBc	44 dBc
≥10 MHz to ≤100 MHz	0.05 V to 0.5 V	53 dBc	48 dBc
	1 V to 5 V	48 dBc	48 dBc

Table 11. ENOB, Nominal[21]

Input Frequency	Input Range (V_{pk-pk})	ENOB
<10 MHz	10 V to 20 V	7.1
≤100 MHz	0.05 V	6.2
	0.1 V	6.8

20. Verified using a 50 Ω source and 50 Ω feedthrough terminator.
21. -1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics. 7.2 kHz resolution bandwidth.
22. Excludes ADC interleaving spurs.

Input Frequency	Input Range (V_{pk-pk})	ENOB
	0.2 V to 5 V	7.1

Noise

Table 12. RMS Noise[23]

Input Impedance	Input Range (V_{pk-pk})	Typical	Warranted
50 Ω [23]	0.05 V	0.55% of FS	0.62% of FS
	0.1 V	0.33% of FS	0.39% of FS
	0.2 V to 5 V	0.28% of FS	0.34% of FS
1 MΩ	0.05 V	0.55% of FS	0.62% of FS
	0.1 V	0.33% of FS	0.39% of FS
	0.2 V to 50 V	0.28% of FS	0.34% of FS

Skew

Channel-to-channel skew	
50 Ω to 50 Ω	<25 ps, nominal
1 MΩ to 1 MΩ	<125 ps, nominal
50 Ω to 1 MΩ	<800 ps, nominal

Horizontal

Sample Clock

Sources

23. Verified using a 50 Ω terminator connected to input.

Internal	Onboard clock (internal VCO)
External	Front panel SMB connector

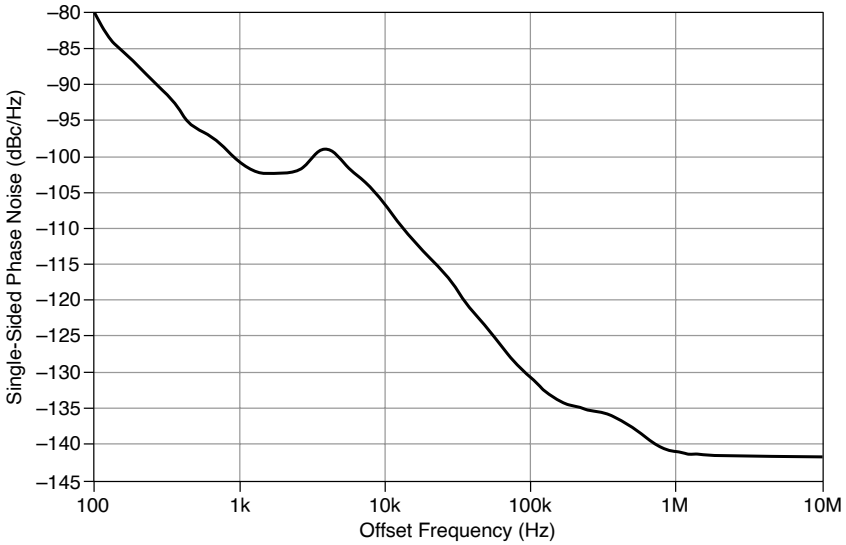
Onboard Clock

Real-time sample rate range[24]	
One channel enabled	76.299 kS/s to 5 GS/s
Two channels enabled[25]	76.299 kS/s to 2.5 GS/s
Four channels enabled	76.299 kS/s to 1.25 GS/s
Random interleaved sampling (RIS) range[26]	Up to 100 GS/s

Figure 9. PXIe-5162 Phase Noise (Plotted without Spurs) at 1 GHz, 3 dBm Input Signal, Locked to

24. Divide by *n* decimation from 1.25 GS/s used for all rates less than 1.25 GS/s. For more information about the Sample Clock and decimation, refer to the *NI High-Speed Digitizers Help*.
25. For the PXIe-5162 (4 CH), supported on channels 0 and 2. For the PXIe-5162 (2 CH), supported on channels 0 and 1.
26. With one channel enabled, stepped in multiples of 5 GS/s. With two channels enabled, stepped in multiples of 2.5 GS/s. With four channels enabled, stepped in multiples of 1.25 GS/s.

Onboard Reference Clock, Measured



Sample Clock jitter[27]	180 fs RMS (12 kHz to 10 MHz), nominal
Timebase frequency	2.5 GHz
Timebase accuracy[28]	±10 ppm, typical ±25 ppm, warranted

Phase-Locked Loop (PLL) Reference Clock

Sources	
Internal	Onboard 10 MHz reference
External	External 10 MHz (front panel CLK IN connector) or PXI_CLK10 (backplane connector)

27. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.
28. When phase-locked to an external Reference Clock, the timebase accuracy is equal to the external Reference Clock accuracy. For example, when locked to the System Reference Clock of a PXI Express chassis, the module inherits the accuracy of the chassis System Reference Clock.

Duty cycle tolerance	45% to 55%

External Sample Clock (CLK IN, Front Panel Connector)

Input voltage range, when configured as a Sample Clock	-10 dBm through 16 dBm
Maximum input overload, when configured as a Sample Clock	18 dBm
Impedance	50 Ω
Coupling	AC
Frequency range	1.25 GHz to 2.5 GHz[29]

External Reference Clock In (CLK IN, Front Panel Connector)

Input voltage range, when configured as a Reference Clock	200 mV_{pk-pk} to 4 V_{pk-pk}
Maximum input overload, when configured as a Reference Clock	5 V_{pk-pk} with |Peaks| ≤10 V
Impedance	50 Ω
Coupling	AC

29. To achieve the same real-time sample rate ranges as the onboard clock, a 2.5 GHz frequency is required.

Frequency range[30]	10 MHz

Reference Clock Out (CLK OUT, Front Panel Connector)

Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	±10 mA

Trigger

Supported trigger	Reference (Stop) Trigger
Trigger types	Edge Digital Immediate Hysteresis Software

Trigger sources	
PXIe-5162 (2 CH)	CH 0, CH 1, TRIG, PFI 0, PFI 1, PXI_TRIG <0..6>, and Software
PXIe-5162 (4 CH)	CH 0, CH 1, CH 2, CH 3, PFI 0, PFI 1, PXI_TRIG <0..6>, and Software

30. The PLL Reference Clock frequency must be accurate to ±25 ppm.

Time-to-digital conversion circuit time resolution	4 ps
Dead time	710 ns, nominal
Holdoff	6.4 ns to 27.4 s
Trigger delay	From 0 to 73,786,976 seconds (28 months), nominal

Analog Trigger (Edge Trigger Type)

Sources	
PXIe-5162 (2 CH)	CH 0, CH 1, or TRIG[31]
PXIe-5162 (4 CH)	CH 0, CH 1, CH 2, or CH 3
Trigger filters	
Low-frequency reject	150 kHz, nominal
High-frequency reject	150 kHz, nominal
Trigger sensitivity	3% of FS at ≤100 MHz, nominal
Trigger accuracy[32]	6% of FS at ≤100 MHz, nominal

31. For specifications on the TRIG input, refer to the *External Trigger (TRIG, Front Panel Connector)* section.

Trigger jitter	4.7 ps

External Trigger (TRIG, Front Panel Connector)

Note TRIG is valid only for the PXIe-5162 (2 CH) device.

Connector	BNC
Impedance	50 Ω or 1 MΩ
Coupling	AC or DC
Input voltage range	
50 Ω	±2.5 V
1 MΩ	±5 V
Maximum input overload	
50 Ω	|Peaks| ≤5 V, nominal
1 MΩ	|Peaks| ≤42 V, nominal
Trigger sensitivity	3% of FS at ≤100 MHz, nominal

32. When the impedance settings of the triggering input and the analog input channel are the same. Delay will increase if the impedance of the triggering input does not match the impedance of the analog input channel.

Trigger accuracy[33]	8% of FS at ≤100 MHz, nominal
Trigger jitter	4.7 ps

Digital Trigger (Digital Trigger Type)

Sources[34]	
Front panel SMB connector	PFI <0..1>
Backplane connector	PXI_TRIG <0..6>

Programmable Function Interface (PFI 0 and PFI 1, Front Panel Connectors)

Connector	SMB jack
Direction	Bidirectional

As an Input (Trigger)

Destinations	Start Trigger (Acquisition Arm) Reference (Stop) Trigger

33. When the impedance settings of the triggering input and the analog input channel are the same. Delay will increase if the impedance of the triggering input does not match the impedance of the analog input channel.
34. Subsample trigger accuracy not supported on PFI 1 or PXI_TRIG<0..6>.

	Advance Trigger
Input impedance	10 kΩ
V_{IH}	2.0 V
V_{IL}	0.8 V
Maximum input overload	-0.5 V to 5.5 V
Maximum frequency	25 MHz

As an Output (Event)

Sources	Ready for Start Start Trigger (Acquisition Arm) Ready for Reference Arm Reference Trigger Reference (Stop) Trigger End of Record Ready for Advance Advance Trigger Done (End of Acquisition) Probe Compensation[35]

Output impedance	50 Ω, nominal
Logic type	3.3 V CMOS
Maximum current drive	±10 mA
Maximum frequency	25 MHz

CableSense

CableSense pulse voltage[36]	0.5 V , nominal
CableSense pulse rise time[37]	650 ps , nominal

Driver support for CableSense on the PXIe-5162 was first available in NI-SCOPE18.7.

Waveform Specifications

Table 13. Waveform Specifications

Onboard memory size	2 GB **Note** Devices with the 154772A-x2L part number had 1 GB of onboard memory.
Minimum record length	1 sample

35. 1 kHz, 50% duty cycle square wave, PFI 1 only.
36. When measured with a high-impedance device.
37. When sourcing into a 50 Ω cable or load.

Number of pretrigger samples	Zero up to full record length
Number of posttrigger samples	Zero up to full record length
Maximum number of records in onboard memory	100,000
Allocated onboard memory per record	[(*Record length* + 448 samples) × 2 bytes/sample], rounded up to an integer multiple of 128 bytes (minimum 512 bytes)

Note

Onboard memory is shared between all enabled channels. You can exceed the maximum number of records in onboard memory if you fetch records while acquiring data. For more information, see *NI High-Speed Digitizers Getting Started Guide*.

The number of pretrigger and posttrigger samples apply to single-record and multirecord acquisitions.

Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, on *ni.com/docs*. You can also find the letter of volatility in the *Related Information* section.

Calibration

External Calibration

External calibration calibrates the onboard references used in self-calibration and the external trigger levels. All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for gain, offset, triggering, and timing errors for all input ranges.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE4.1.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-5162. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW

- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)
- Python (*pypi.org/project/niscope*)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PXIe-5162 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.

Note InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

Interactive control of the PXIe-5162 was first available via InstrumentStudio in NI-SCOPE 18.1 and via the NI-SCOPE SFP in NI-SCOPE 4.1. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5162. MAX is included on the driver media.

TClk Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help*, which is located within the *NI High-Speed Digitizers Help*. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

Intermodule SMC Synchronization Using NI-TClk for Identical Modules

Specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample clocks of each module.
- All parameters are set to identical values for each SMC-based module.
- Modules are synchronized without using an external Sample clock.
- Self-calibration is completed.

Note Although you can use NI-TClk to synchronize non-identical SMC-based modules, these specifications apply only to synchronizing identical modules.

Skew[38]	100 ps, nominal
Skew after manual adjustment	≤5 ps, nominal
Sample clock delay/adjustment resolution	20 fs

Power Requirements

+3.3 VDC	2.2 A, nominal
+12 VDC	2.3 A, nominal
Total power	34.8 W, nominal

Physical Characteristics

Dimensions	3U, 1 slot, PXI Express gen 1 x4 Module

38. Caused by clock and analog path delay differences. No manual adjustment performed. Tested with a NI PXIe-1082 chassis with a maximum slot-to-slot skew of 100 ps.

	21.4 cm × 2.0 cm × 13.1 cm (8.4 in. × 0.8 in. × 5.1 in.)
Weight	430 g (15 oz.)

Environmental Characteristics

Table 14. Temperature

Operating	0 °C to 45 °C
Storage	-40 °C to 71 °C

Table 15. Humidity

Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing

Table 16. Pollution Degree

Pollution degree	2

Table 17. Maximum Altitude

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)

Table 18. Shock and Vibration

Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse