PXIe-5162 Specifications

2026-09-01

Contents

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These specifications apply to the PXIe-5162.

Revision History

Version	Date changed	Description
373858M-01	September 2026	Added 1 GB onboard memory variant.
373858L-01	March 2026	Removed 64 MB onboard memory variant.
373858K-01	January 2025	Added pinouts
373858G-01	March 2018	Renamed to PXIe-5162.
375320A-01	December 2012	Initial release.

Looking For Something Else?

For information not found in the specifications for your product, such as operating instructions, browse *Related Information*.

Related information:

- PXIe-5162 User Manual
- PXIe-5162 Calibration Procedure
- NI-SCOPE User Manual
- Software and Driver Downloads
- PXIe-5162 Dimensional Drawings
- PXIe-5162 Product Certifications
- PXIe-5160/5162 Letter of Volatility
- Discussion Forums

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. *Warranted* specifications account for measurement uncertainties, temperature drift, and aging. *Warranted* specifications are ensured by design, or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured (meas)* specifications describe the measured performance of a representative model.

Specifications are *Typical* unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges
- All bandwidths and bandwidth limit filters
- Sample rate set to 1.25 GS/s, 2.5 GS/s, or 5 GS/s
- Onboard Sample clock locked to onboard Reference clock

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature ranges of 0 °C to 45 °C
- The PXIe-5162 is warmed up for 15 minutes at ambient temperature
- Self-calibration is completed after warm-up period
- Calibration cycle is maintained
- The PXI Express chassis fan speed is set to HIGH, the foam fan filters are removed if present, and the empty slots contain PXI chassis slot blockers and filler panels. For more information about cooling, refer to the Maintain Forced-Air Cooling Note to

Users document available at ni.com/docs.
- NI-SCOPE 4.1 or later instrument driver is used
- External calibration is performed at 23 °C ± 3 °C

Typical specifications are valid under the following conditions unless otherwise noted:

- Ambient temperature ranges of 0 °C to 45 °C

PXIe-5162 Pinout

Use the pinout to connect to terminals on the PXIe-5162.

Figure 1. PXIe-5162 Connector Pinout

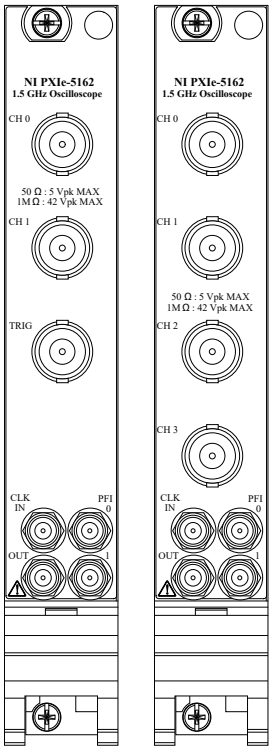


Table 1. PXIe-5162 (2CH) Front Panel Connectors

Label	Function	Connector Type
CH 0 and CH 1	Analog input connection; digitizes data and triggers acquisitions.	BNC female
TRIG	External analog trigger; signals on the TRIG connector cannot	BNC female

Label	Function	Connector Type
	be digitized.	
CLK IN	Imports an external Reference Clock or Sample Clock to the device.	SMB jack
CLK OUT	Exports the Reference Clock from the device.	SMB jack
PFI 0	PFI line for digital trigger input/output.	SMB jack
PFI 1	PFI line for digital trigger input/output and probe compensation. No subsample trigger accuracy.	SMB jack

Table 2. PXIe-5162 (4CH) Front Panel Connectors

Label	Function	Connector Type
CH 0 to CH 3	Analog input connection; digitizes data and triggers acquisitions.	BNC female
CLK IN	Imports an external Reference Clock or Sample Clock to the device.	SMB jack
CLK OUT	Exports the Reference Clock from the device.	SMB jack
PFI 0	PFI line for digital trigger input/output.	SMB jack
PFI 1	PFI line for digital trigger input/output and probe compensation. No subsample trigger accuracy.	SMB jack

Vertical

Analog Input

Table 3. Number of Channels

Parameter	Value
PXIe-5162 (2 CH)	Two (simultaneously sampled)
PXIe-5162 (4 CH)	Four (simultaneously sampled)

Table 4. Input

Parameter	Value
Input type	Referenced single-ended
Connectors	BNC

Impedance and Coupling

Note You can configure the impedance and coupling settings for each channel independently in software.

Table 5. Input Impedance

Impedance Setting	Typical	Warranted
50 Ω	50 Ω ± 1.50%	50 Ω ± 1.75%
1 MΩ	1 MΩ ± 0.75%	1 MΩ ± 0.90%

Table 6. Input Capacitance

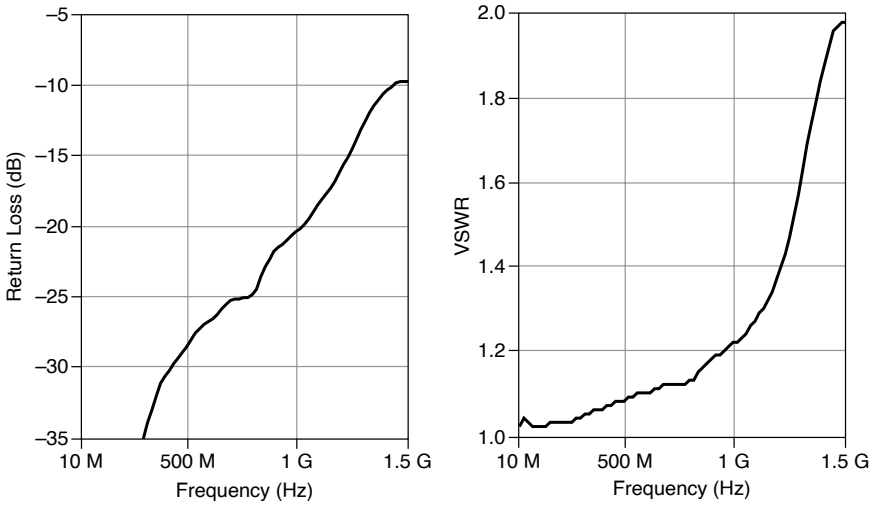
Parameter	Nominal	Warranted
Input capacitance[1]	15 pF ± 0.8 pF	15 pF ± 2.5 pF

Table 7. Input Coupling

Parameter	Value
Input coupling	AC, DC

1. 1 MΩ input only.

Figure 2. 50 Ω Input Return Loss and Input VSWR, Measured



Voltage Levels

Table 8. 50 Ω Full-Scale (FS) Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	**Vertical Offset Range (V)**
0.05 V	±0.5
0.1 V	±0.5
0.2 V	±0.5
0.5 V	±0.5
1 V	±0.5
2 V	±1.5
5 V	0

Table 9. 1 MΩ FS Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	**Vertical Offset Range (V)**
0.05 V	±0.5
0.1 V	±0.5
0.2 V	±0.5
0.5 V	±0.5
1 V	±0.5
2 V	±5

Input Range (V_{pk-pk})	Vertical Offset Range (V)
5 V	±5
10 V	±5
20 V	±30
50 V	±15

Table 10. Maximum Input Overload

Impedance Setting	Maximum Input Overload
50 Ω	|Peaks| ≤5 V, nominal
1 MΩ	|Peaks| ≤42 V, nominal

Notice Signals exceeding the maximum input overload may damage the device.

Accuracy

Parameter	Value
Resolution	10 bits
DC accuracy[2]	±[(2% × |*Reading* - *Vertical Offset*|) + (1.4% × |*Vertical Offset*|) + (0.6% of *FS*) + 600 µV]
DC drift[3]	±[(0.1% × |*Reading* - *Vertical Offset*|) + (0.025% × |*Vertical Offset*|) + (0.03% of *FS*)] per °C, nominal
AC amplitude accuracy[4]	±0.5 dB at 50 kHz
AC amplitude drift[5]	±0.01 dB per °C at 50 kHz, nominal

2. Within ±3 °C of self-calibration temperature. This specification is *typical* for peak-to-peak input ranges of 0.05 V to 0.1 V and *warranted* for all other input ranges.
3. Used to calculate errors when onboard temperature changes more than ±3 °C from the self-calibration temperature.
4. Within ±3 °C of self-calibration temperature. This specification is *typical* for peak-to-peak input ranges of 0.05 V to 0.1 V and *warranted* for all other input ranges.
5. Used to calculate errors when onboard temperature changes more than ±3 °C from the self-calibration temperature.

Table 11. Channel-to-Channel Crosstalk, Nominal[6]

Input Impedance	Input Frequency	Crosstalk
50 Ω	DC ≤ *f* ≤ 100 MHz	-60 dB
	100 MHz < *f* ≤ 700 MHz	-45 dB
	700 MHz < *f* ≤ 1000 MHz	-40 dB
1 MΩ[7]	DC ≤ *f* ≤ 100 MHz	-55 dB
	100 MHz < *f* ≤ 200 MHz	-45 dB

Bandwidth and Transient Response

Table 12. 50 Ω Bandwidth (-3 dB)[8]

Input Impedance	Value
50 Ω bandwidth	1.5 GHz, warranted

Table 13. 1 MΩ Bandwidth (-3 dB)[9]

Input Impedance	Input Range (V_{pk-pk})	Nominal	Warranted
1 MΩ[10]	0.05 V to 1 V	—	300 MHz
	2 V to 10 V	300 MHz	250 MHz[11]
	20 V to 50 V	300 MHz	—

Table 14. Bandwidth-Limiting Filters[12]

Parameter	Value
Bandwidth-limiting filters	20 MHz and 175 MHz

6. Measured on one channel with test signal applied to another channel with the same range setting on both channels.
7. Only valid on peak-to-peak input ranges of 0.05 V to 10 V.
8. Normalized to 50 kHz.
9. Normalized to 50 kHz.
10. Verified using a 50 Ω source and 50 Ω feed-through terminator.
11. For ambient temperature ranges of 0 °C to 30 °C.
12. Normalized to 50 kHz.

Table 15. Rise/Fall Time[13]

Input Impedance	Rise/Fall Time
50 Ω	320 ps
1 MΩ[14]	1.4 ns

Table 16. AC-Coupling Cutoff (-3 dB)[15]

Input Impedance	AC-Coupling Cutoff
50 Ω[16]	170 kHz
1 MΩ	17 Hz

Figure 3. PXIe-5162 Step Response, 50 Ω, 1 V_{pk-pk} Input Range, -0.25 V Programmable Offset, 150 ps Rising Edge, Measured

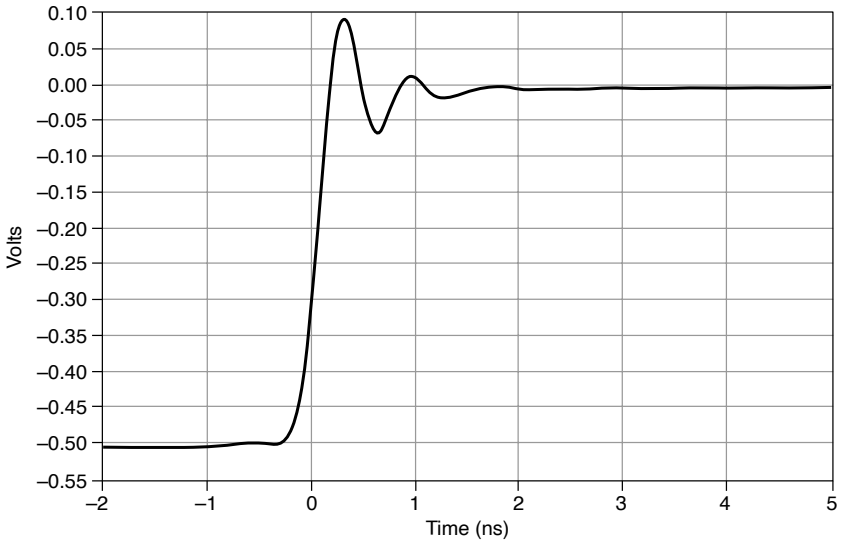


Figure 4. PXIe-5162 Step Response, 1 MΩ, 1 V_{pk-pk} Input Range, -0.25 V Programmable Offset, 500 ps

13. 50% FS input pulse.
14. Verified using a 50 Ω source and 50 Ω feed-through terminator.
15. Verified using a 50 Ω source.
16. With AC coupling enabled, the DC resistance to ground is 20 kΩ.

Rising Edge, Measured[17]

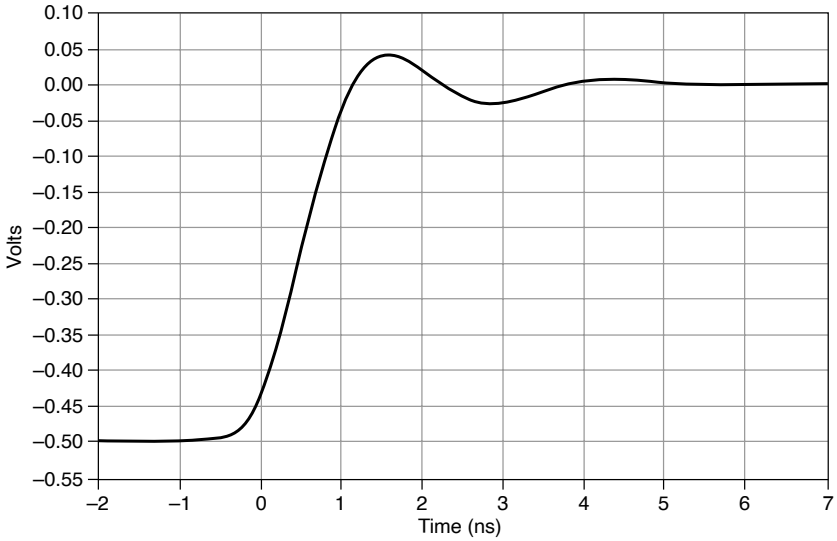
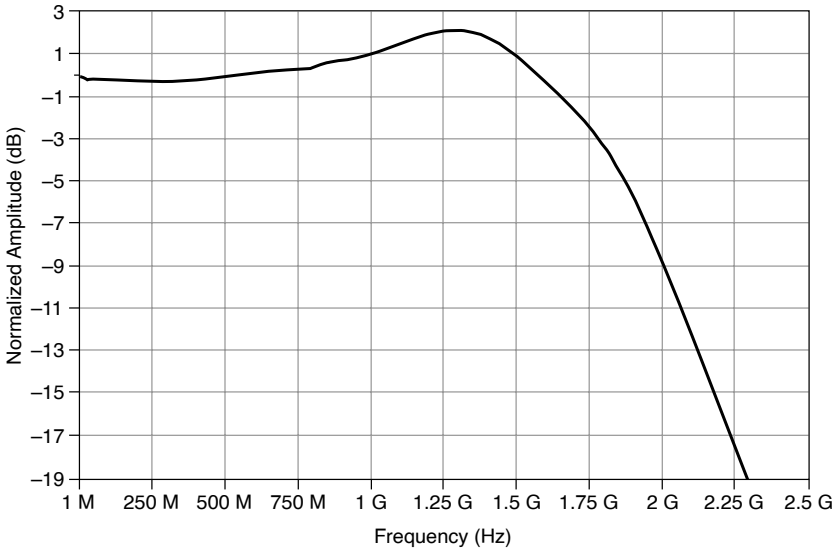


Figure 5. PXIe-5162 50 Ω Frequency Response, 1 V_{pk-pk}, 5 GS/s, Measured



17. Verified using a 50 Ω source and 50 Ω feed-through terminator.

Figure 6. PXIe-5162 1 MΩ Frequency Response, 1 V_{pk-pk}, Measured[18]

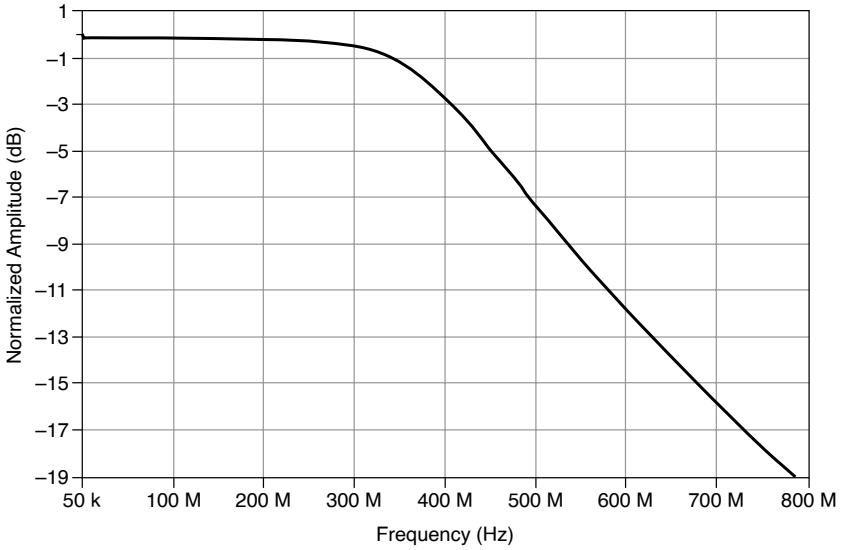
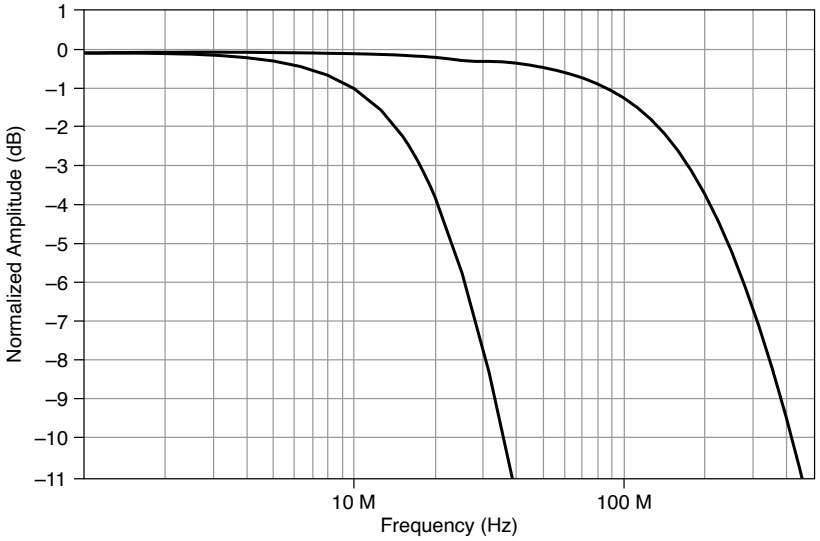


Figure 7. PXIe-5162 Bandwidth-Limiting Filters Frequency Response, 1 V_{pk-pk}, Measured



18. Verified using a 50 Ω source and 50 Ω feed-through terminator.

Spectral Characteristics

50 Ω Spectral Characteristics

Table 17. Spurious-Free Dynamic Range (SFDR), Measured[19]

Input Frequency	Input Range (V_{pk-pk})	SFDR	
		1.25 GS/s, 2.5 GS/s[20], 5.0 GS/s[21]	2.5 GS/s, 5.0 GS/s
<10 MHz	0.05 V	52 dBc	40 dBc
	0.1 V	52 dBc	46 dBc
	0.2 V	56 dBc	46 dBc
	0.5 V to 5 V	56 dBc	50 dBc
≥10 MHz to ≤1 GHz	0.05 V	46 dBc	40 dBc
	0.1 V to 5 V	46 dBc	46 dBc

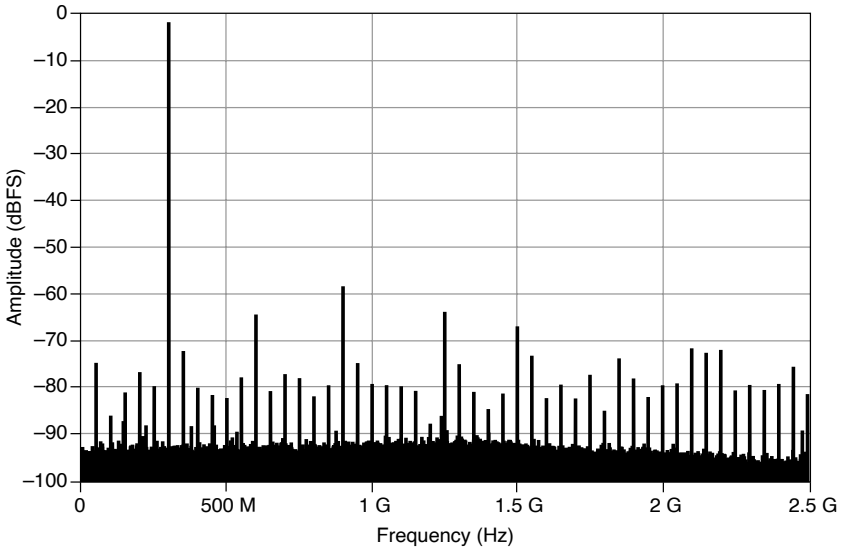
Table 18. Effective Number of Bits (ENOB), Nominal[22]

Input Frequency	Input Range (V_{pk-pk})	ENOB
<1 GHz	0.05 V	6.0
	0.1 V	6.6
	0.2 V to 5 V	7.0

Figure 8. PXIe-5162 Single-Tone Spectrum, 2.98 dBm Input Signal at Connector, 50 Ω, 1 V_{pk-pk}, 5 GS/s,

19. -1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics. 7.2 kHz resolution bandwidth.
20. Excludes ADC interleaving spurs.
21. Excludes ADC interleaving spurs.
22. -1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics. 7.2 kHz resolution bandwidth.

300 MHz Input Tone, Full Bandwidth, Measured



1 MΩ Spectral Characteristics[23]

Table 19. SFDR, Nominal[24]

Input Frequency	Input Range (V_{pk-pk})	SFDR	
		1.25 GS/s, 2.5 GS/s[25], 5.0 GS/s[26]	2.5 GS/s, 5.0 GS/s
<10 MHz	0.05 V to 10 V	53 dBc	48 dBc
	20 V	50 dBc	44 dBc
≥10 MHz to ≤100 MHz	0.05 V to 0.5 V	53 dBc	48 dBc
	1 V to 5 V	48 dBc	48 dBc

Table 20. ENOB, Nominal[27]

Input Frequency	Input Range (V_{pk-pk})	ENOB
<10 MHz	10 V to 20 V	7.1
≤100 MHz	0.05 V	6.2

23. Verified using a 50 Ω source and 50 Ω feedthrough terminator.
24. -1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics. 7.2 kHz resolution bandwidth.
25. Excludes ADC interleaving spurs.
26. Excludes ADC interleaving spurs.
27. -1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics. 7.2 kHz resolution bandwidth.

Input Frequency	Input Range (V_{pk-pk})	ENOB
	0.1 V	6.8
	0.2 V to 5 V	7.1

Noise

Table 21. RMS Noise[28]

Input Impedance	Input Range (V_{pk-pk})	Typical	Warranted
50 Ω	0.05 V	0.55% of FS	0.62% of FS
	0.1 V	0.33% of FS	0.39% of FS
	0.2 V to 5 V	0.28% of FS	0.34% of FS
1 MΩ	0.05 V	0.55% of FS	0.62% of FS
	0.1 V	0.33% of FS	0.39% of FS
	0.2 V to 50 V	0.28% of FS	0.34% of FS

Skew

Table 22. Channel-to-Channel Skew

Parameter	Value
50 Ω to 50 Ω	<25 ps, nominal
1 MΩ to 1 MΩ	<125 ps, nominal
50 Ω to 1 MΩ	<800 ps, nominal

Horizontal

Sample Clock

Table 23. Sample Clock Sources

Source Type	Source
Internal	Onboard clock (internal VCO)
External	Front panel SMB connector

28. Verified using a 50 Ω terminator connected to input.

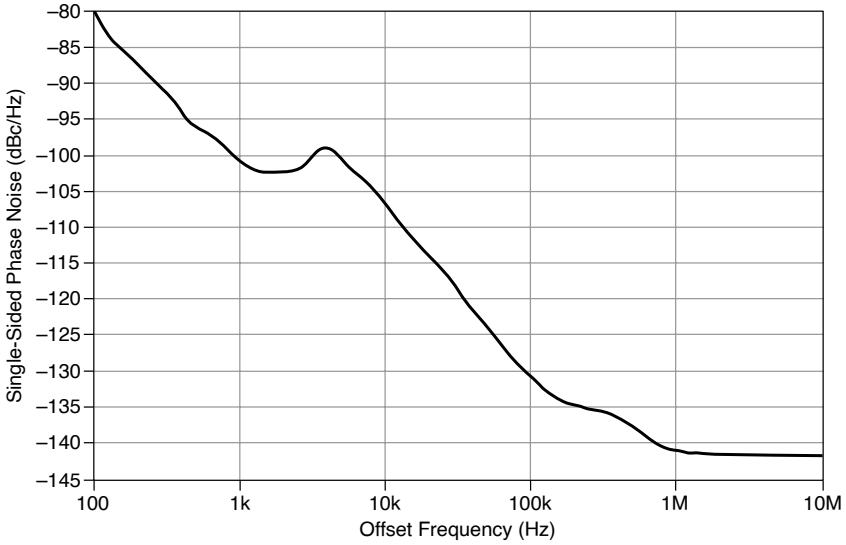
Onboard Clock

Table 24. Real-time Sample Rate Range[29]

Number of Channels Enabled	Real-time Sample Rate Range
One channel	76.299 kS/s to 5 GS/s
Two channels[30]	76.299 kS/s to 2.5 GS/s
Four channels	76.299 kS/s to 1.25 GS/s

Parameter	Value
Random interleaved sampling (RIS) range[31]	Up to 100 GS/s

Figure 9. PXIe-5162 Phase Noise (Plotted without Spurs) at 1 GHz, 3 dBm Input Signal, Locked to Onboard Reference Clock, Measured



Parameter	Value
Sample Clock jitter[32]	180 fs RMS (12 kHz to 10 MHz), nominal

29. Divide by *n* decimation from 1.25 GS/s used for all rates less than 1.25 GS/s. For more information about the Sample Clock and decimation, refer to the *NI-SCOPE User Manual*.
30. For the PXIe-5162 (4 CH), supported on channels 0 and 2. For the PXIe-5162 (2 CH), supported on channels 0 and 1.
31. With one channel enabled, stepped in multiples of 5 GS/s. With two channels enabled, stepped in multiples of 2.5 GS/s. With four channels enabled, stepped in multiples of 1.25 GS/s.
32. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes

Parameter	Value
Timebase frequency	2.5 GHz
Timebase accuracy[33]	±10 ppm, typical ±25 ppm, warranted

Phase-Locked Loop (PLL) Reference Clock

Table 25. PLL Reference Clock Sources

Source Type	Source
Internal	Onboard 10 MHz reference
External	External 10 MHz (front panel CLK IN connector) or PXI_CLK10 (backplane connector)

Table 26. Duty Cycle Tolerance

Parameter	Value
Duty cycle tolerance	45% to 55%

External Sample Clock (CLK IN, Front Panel Connector)

Table 27. External Sample Clock Specifications

Parameter	Value
Input voltage range, when configured as a Sample Clock	-10 dBm through 16 dBm
Maximum input overload, when configured as a Sample Clock	18 dBm
Impedance	50 Ω
Coupling	AC
Frequency range	1.25 GHz to 2.5 GHz[34]

trigger jitter.

33. When phase-locked to an external Reference Clock, the timebase accuracy is equal to the external Reference Clock accuracy. For example, when locked to the System Reference Clock of a PXI Express chassis, the module inherits the accuracy of the chassis System Reference Clock.

External Reference Clock In (CLK IN, Front Panel Connector)

Table 28. External Reference Clock In Specifications

Parameter	Value
Input voltage range, when configured as a Reference Clock	200 mV_{pk-pk} to 4 V_{pk-pk}
Maximum input overload, when configured as a Reference Clock	5 V_{pk-pk} with |Peaks| ≤10 V
Impedance	50 Ω
Coupling	AC
Frequency range[35]	10 MHz

Reference Clock Out (CLK OUT, Front Panel Connector)

Table 29. Reference Clock Out Specifications

Parameter	Value
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	±10 mA

Trigger

Table 30. Trigger Specifications

Parameter	Value
Supported trigger	Reference (Stop) Trigger
Trigger types	Edge, Digital, Immediate, Hysteresis, and Software
Time-to-digital conversion circuit time	4 ps

34. To achieve the same real-time sample rate ranges as the onboard clock, a 2.5 GHz frequency is required.
35. The PLL Reference Clock frequency must be accurate to ±25 ppm.

Parameter	Value
resolution	
Dead time	710 ns, nominal
Holdoff	6.4 ns to 27.4 s
Trigger delay	From 0 to 73,786,976 seconds (28 months), nominal

Table 31. Trigger Sources

Model	Trigger Sources
PXIe-5162 (2 CH)	CH 0, CH 1, TRIG, PFI 0, PFI 1, PXI_TRIG <0..6>, and Software
PXIe-5162 (4 CH)	CH 0, CH 1, CH 2, CH 3, PFI 0, PFI 1, PXI_TRIG <0..6>, and Software

Analog Trigger (Edge Trigger Type)

Table 32. Analog Trigger Sources

Model	Analog Trigger Sources
PXIe-5162 (2 CH)	CH 0, CH 1, or TRIG[36]
PXIe-5162 (4 CH)	CH 0, CH 1, CH 2, or CH 3

Table 33. Analog Trigger Filters

Parameter	Value
Low-frequency reject	150 kHz, nominal
High-frequency reject	150 kHz, nominal

Table 34. Analog Trigger Sensitivity, Accuracy, and Jitter

Parameter	Value
Trigger sensitivity	3% of FS at ≤100 MHz, nominal
Trigger accuracy[37]	6% of FS at ≤100 MHz, nominal

36. For specifications on the TRIG input, refer to the *External Trigger (TRIG, Front Panel Connector)* section.
37. When the impedance settings of the triggering input and the analog input channel are the same. Delay will increase if the impedance of the triggering input does not match the impedance of the analog input channel.

Parameter	Value
Trigger jitter	4.7 ps

External Trigger (TRIG, Front Panel Connector)

Note TRIG is valid only for the PXIe-5162 (2 CH) device.

Table 35. External Trigger Specifications

Parameter	Value
Connector	BNC
Impedance	50 Ω or 1 MΩ
Coupling	AC or DC
Trigger sensitivity	3% of FS at ≤100 MHz, nominal
Trigger accuracy[38]	8% of FS at ≤100 MHz, nominal
Trigger jitter	4.7 ps

Table 36. Input Voltage Range

Impedance	Input Voltage Range
50 Ω	±2.5 V
1 MΩ	±5 V

Table 37. Maximum Input Overload

Impedance	Maximum Input Overload
50 Ω	|Peaks| ≤5 V, nominal
1 MΩ	|Peaks| ≤42 V, nominal

38. When the impedance settings of the triggering input and the analog input channel are the same. Delay will increase if the impedance of the triggering input does not match the impedance of the analog input channel.

Digital Trigger (Digital Trigger Type)

Table 38. Sources[39]

Connector	Sources
Front panel SMB connector	PFI <0..1>
Backplane connector	PXI_TRIG <0..6>

Programmable Function Interface (PFI 0 and PFI 1, Front Panel Connectors)

Table 39. PFI Connector Specifications

Parameter	Value
Connector	SMB jack
Direction	Bidirectional

Table 40. PFI as an Input (Trigger)

Parameter	Value
Destinations	• Start Trigger (Acquisition Arm) • Reference (Stop) Trigger • Advance Trigger
Input impedance	10 kΩ
V_{IH}	2.0 V
V_{IL}	0.8 V
Maximum input overload	-0.5 V to 5.5 V
Maximum frequency	25 MHz

39. Subsample trigger accuracy not supported on PFI 1 or PXI_TRIG<0..6>.

Table 41. PFI as an Output (Event)

Parameter	Value
Sources	• Ready for Start • Start Trigger (Acquisition Arm) • Ready for Reference • Arm Reference Trigger • Reference (Stop) Trigger • End of Record • Ready for Advance • Advance Trigger • Done (End of Acquisition) • Probe Compensation[40]
Output impedance	50 Ω, nominal
Logic type	3.3 V CMOS
Maximum current drive	±10 mA
Maximum frequency	25 MHz

CableSense

Table 42. CableSense Pulse Voltage and Rise Time

Parameter	Value
CableSense pulse voltage[41]	0.5 V, nominal
CableSense pulse rise time[42]	650 ps, nominal

Driver support for CableSense on the PXIe-5162 was first available in NI-SCOPE 18.7. To learn more about CableSense technology, visit *Avoid Test System Downtime With CableSense Technology*.

40. 1 kHz, 50% duty cycle square wave, PFI 1 only.
41. When measured with a high-impedance device.
42. When sourcing into a 50 Ω cable or load.

Waveform Specifications

Table 43. Waveform Specifications

Parameter	Value
Onboard memory size	1 GB or 2 GB **Note** Devices with the 154772A-x2L part number had 1 GB of onboard memory.
Minimum record length	1 sample
Number of pretrigger samples	Zero up to full record length
Number of posttrigger samples	Zero up to full record length
Maximum number of records in onboard memory	100,000
Allocated onboard memory per record	[(*Record length* + 448 samples) × 2 bytes/sample], rounded up to an integer multiple of 128 bytes (minimum 512 bytes)

Note

Onboard memory is shared between all enabled channels. You can exceed the maximum number of records in onboard memory if you fetch records while acquiring data. For more information, see *NI High-Speed Digitizers Getting Started Guide*.

The number of pretrigger and posttrigger samples apply to single-record and multirecord acquisitions.

Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, on *ni.com/docs*. You can also find the letter of volatility in the *Related*

Information section.

Calibration

External calibration calibrates the onboard references used in self-calibration and the external trigger levels. All calibration constants are stored in nonvolatile memory.

Self-calibration is done on software command. The calibration corrects for gain, offset, triggering, and timing errors for all input ranges.

Table 44. Calibration Specifications

Parameter	Value
Interval for external calibration	2 years
Warm-up time	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE 4.1.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-5162. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)
- Python (*pypi.org/project/niscope*)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PXIe-5162 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.

Note InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

Interactive control of the PXIe-5162 was first available via InstrumentStudio in NI-SCOPE 18.1 and via the NI-SCOPE SFP in NI-SCOPE 4.1. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5162. MAX is included on the driver media.

TClk Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk User Manual*. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

Intermodule SMC Synchronization Using NI-TClk for Identical Modules

Specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample clocks of each module.
- All parameters are set to identical values for each SMC-based module.
- Modules are synchronized without using an external Sample clock.
- Self-calibration is completed.

Note Although you can use NI-TClk to synchronize non-identical SMC-based modules, these specifications apply only to synchronizing identical modules.

Table 45. NI-TClk Intermodule Synchronization Specifications

Parameter	Value
Skew[43]	100 ps, nominal
Skew after manual adjustment	≤5 ps, nominal
Sample clock delay/ adjustment resolution	20 fs

Power Requirements

Table 46. Power Requirements

Parameter	Value
+3.3 V DC	2.2 A, nominal
+12 V DC	2.3 A, nominal
Total power	34.8 W, nominal

Physical Characteristics

Table 47. Physical Characteristics

Parameter	Value
Dimensions	3U, 1 slot, PXI Express gen 1 x4 Module21.4 cm × 2.0 cm × 13.1 cm(8.4 in. × 0.8 in. × 5.1 in.)
Weight	430 g (15 oz.)

43. Caused by clock and analog path delay differences. No manual adjustment performed. Tested with a PXIe-1082 chassis with a maximum slot-to-slot skew of 100 ps.

Environmental Characteristics

Table 48. Temperature

Parameter	Value
Operating temperature	0 °C to 45 °C
Storage temperature	-40 °C to 71 °C

Table 49. Humidity

Parameter	Value
Operating humidity	10% to 90%, non-condensing
Storage humidity	5% to 95%, non-condensing

Table 50. Pollution Degree

Parameter	Value
Pollution Degree	2

Table 51. Maximum Altitude

Parameter	Value
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)

Table 52. Shock and Vibration

Parameter	Value
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse