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# CS548 Isolated Channel Oscilloscope Series Datasheet


The CS548 is an **individually 2 $kV_{DC}$ isolated 4 channel high CMRR oscilloscope with 14 bit resolution, 500 Msps and 200 MHz BW**. It is designed to measure all signals in an operating full or three phase power electronic switching bridge on both the low and high sides down to a few nanoseconds rise and fall times precisely with highest signal fidelity. Applications include gate drives to measure voltage and charge, the power switch to measure loss and parasitic stress, the output to measure power and spectrum for EMC compliance, and the control system for Gain/Phase and stability. All CS5X8 models include an **isolated DC to 65 MHz Signal Generator, 8 Isolated Digital Inputs** and **optional Isolated Digital Outputs** that can be used for **Double Pulse** and **PWM**, combing source and measurement unit together in one compact and clever device. The system can be configured with multiple extensions including **Remote Digitizers** with fibers up to 30 m for making measurements at even higher isolation voltages. For the most demanding applications up to four CS548 can be linked to **make a 16 channel isolated oscilloscope system**, with coherent sampling.

## Front

### Chan A - Chan D local and remote inputs:

- 2 $kV_{DC}$, 1 $kV_{AC}$ CAT II, 600 $V_{AC}$ CAT III operating isolation voltage to ground and other channels. (Local)
- 30 kV operating isolation voltage to ground and other channels, via CS1200 Remote Probe
- 100 dB CMRR at 50 MHz
- 14 bit resolution, 100dB dynamic range
- 200 MHz Analog BW
- 20 pF to chassis
- Two hardware ranges:
  ±0.8 V with 100 µV resolution
  ±8 V with 1 mV resolution
- 200 $\mu V_{RMS}$ noise on 0.8 V range
- probe isolators for protection

### Pod 1 & 2 expansion

- 5 x Bidirectional 400 Mbps LVDS channels per pod
- **CS1301** Isolated digital input pods included.
- **Optional Pods:**
  **CS1302** Isolated four digital outputs + one input.
- **Pulse Builder** for Pulse Trains, PWM, and double pulse generation

### CS1200/CS1201 Remote Digitizers

- Remote fibre connected digitizer head up to 30 meters from CS548.

### Pulse generator/Probe Comp

- Probe Comp output ~ 1 ns rise, fall -time, programmable 5 – 12 V level
- Variable output frequency 50 mHz – 75.3 MHz
- Programmable Pulse train, PWM or Double Pulse

### Calibration

- Programmable DC Cal output for complete probe and channel DC calibration. Ref is 7.5 V or 0.6818 V ± 0.035 %, or short to ground.


## Back

**Signal Generator:**

- Isolated 600 $V_{DC}$, 300 $V_{AC}$ CAT II
- DC - 65 MHz
- 12 bit DAC
- ± 3,5 $V_{p-p}$
- 14 pF to chassis
- 100 dB CMRR at 50 MHz
- Sine, square, arbitrary (incl. patterns)* 100 $\mu V_{RMS}$ noise

**Link Port:**

- Links to CS1070 0-50 MHz 1 A power amplifier, CS1133 $V_{SAT}$ probe.
- Includes UART, SPI and I2C I/O*

**Ethernet:***

- SFP socket based
- Copper 10/100/1000 Mbps
- Fibre 1Gbps

**USB:**

- USB 3-C socket
- USB3 @ 130 MB/s
- USB2 @ 30 MB/s

**Link In/Out:**

- Used to daisy chain multiple units
- Synchronous sample clock
- Trigger and control

**Triggering**

- Two FPGA mixed signal triggers
- Triggers interpolate in time for higher trigger accuracy.
- Triggers may be combined using AND/OR/XOR
- Triggers may be sequences Trigger 1 [num occurrences] - time specification - Trigger 2 [num occurrences]. The time specification is less than a period, in a period range or more than a period. Triggers may be completely independent.
- The digital portion may be rising or falling digital input, conditional on one or more other digital inputs being 0, 1 or don't care. Bit's may be OR'd or AND'd.
- The analog trigger may be conditional on a digital state.

**Power Button**

- Push On- Push Off power button.
- Rear 2 pin connector for remote power or power at start operation.

**Power In:**

- 10 - 24 $V_{DC}$, 43 W.
- Can be car power supply connected, withstands crank and load dump.

## *CS548 Standard Accessories*

The CS548 includes 1 off 1x/10x probe, 100x probe and Common Mode Choke per installed channel, 2 off CS1301 Input Pods, USB Cable, Power Supply, SMA-BNC adaptor, Ethernet SFP module (copper or fibre).

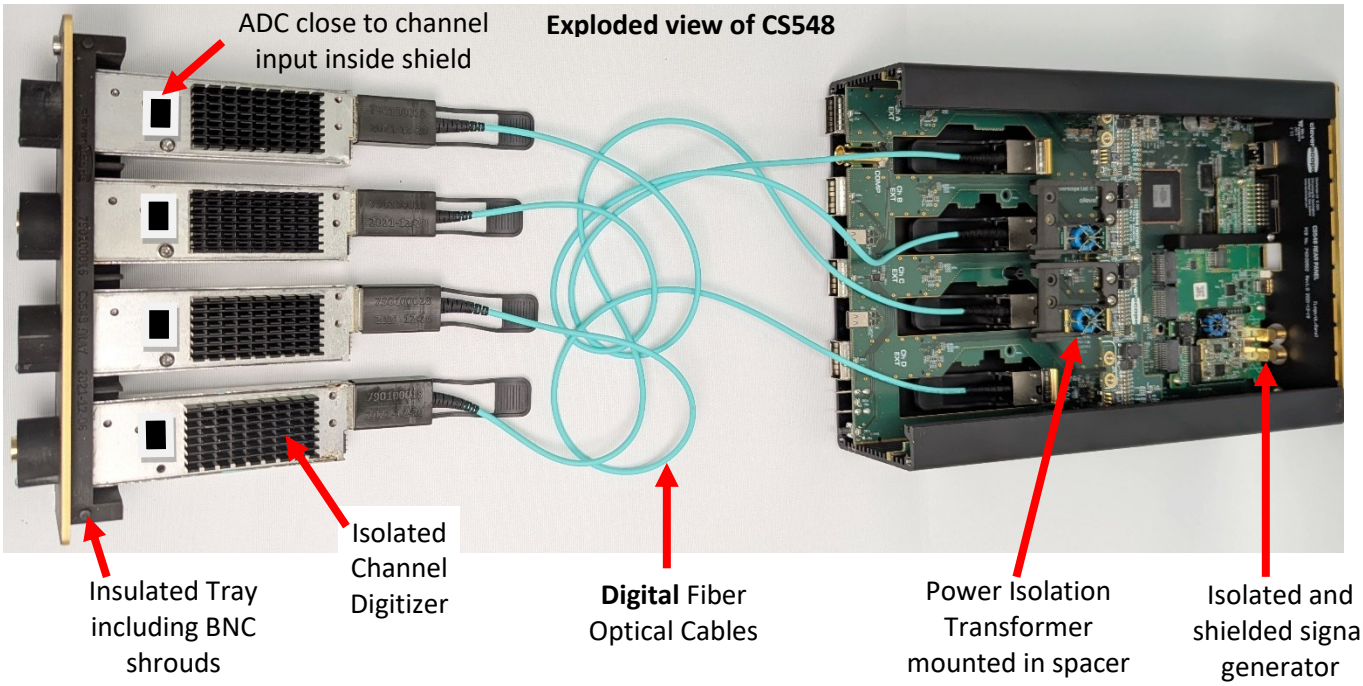
Notes:

* Item still to be implemented. See Specification Status section.

# CS548 Channel Isolation

The CS548 digitizers are held in a plastic insulator tray to maximize creepage and clearance. The tray has a CTI >600 and conforms to Materials Group 1 in the IEC61010-2 standard. We build for use in Pollution Degree 2 environments (only non-conductive pollution occurs except that occasionally a temporary conductivity caused by condensation is expected). The CS548 is for use with up to 600 $V_{AC}$ Category III circuits (permanently connected to the mains switchboard via a fuse).

Each shielded channel digitizer is completely separate and attached to the digitizer power board using a spacer for high CMRR and isolation. The plastic / transformer former (CTI >600) provide a creepage >22 mm and clearance > 18 mm. The low capacitance transformers use triple insulated Rubadue wire (T32A01T5XX-1.5). The Digital Fiber Optical Cable link to the Main board (500mm) has a breakdown voltage >30kV. Each channel is isolated from the chassis and other channels using high dielectric Formex GK-10 (16 kV BV, 600 V CTI) plastic sheets.




We have built the CS548 with the assumption that the UUT is powered by a line to neutral mains voltage <600 $V_{AC}$ and includes secondary circuit working voltages of <2 $kV_{DC}$ or $V_{AC\text{-}PEAK}$. This is measurement category III. These standards apply:

**Clearance:**

- IEC61010-1 (ed 3.0) Table K.11, Reinforced = 2 x 6.9 mm = 13.8 mm
- IEC61010-2-030 Ed 1.0 (Test Equipment), Table K.101, a reinforced insulation clearance: 10.5 mm.
  We use 18 mm.

**Creepage:**

- IEC61010-1 (ed 3.0) Table K.13, 2000 $V_{DC}$, Reinforced = 2 x 10 mm = 20 mm.
  We use 22 mm.

# Warnings

The Isolated Analog Inputs **CHAN A..D** and **SIG GEN** outputs may have high common voltages applied to the coaxial connectors.
**Do NOT touch any connectors connected to the Channels or Sig Gen during operation.** Ensure all connected voltage sources are turned off before changing any connector. Verify this using a multimeter.

The **CHAN A..D** inputs are rated at a maximum of 2 $kV_{DC}$ common mode to real earth, and 1 kV signal to BNC common. **Do NOT exceed these values**.

The **SIG GEN** output is rated at 300VAC CAT II or 600VDC between the coaxial connector common and real earth. **Do NOT exceed this value**.

Link In and Link Out ports on the back side are **NOT** for remote display connection. Use only Cleverscope approved Link Cables for Multi-Unit Synchronisation!

Pod 1 and Pod 2 connectors are **NOT** for USB-C type cables! Only use Cleverscope approved pod cables!

Do NOT allow liquids to enter the CS548.

Do NOT block the CS548 ventilation holes, including placing the CS548 upside down.

Do NOT exceed an input supply voltage of 30 $V_{DC}$.Only power by an external limited energy source (LPS or Class2 power supply), such as the mains power adaptor supplied with the unit.

If the CS548 equipment is used in a manner not specified by Cleverscope, the protection provided by the equipment may be impaired. For example, safety will be impaired if exposed metal connectors are used.

If cleaning the CS548, use only a damp cloth to wipe down any surfaces. Do NOT use IPA or alcohol based products.

# Certifications

The CS548 has been tested to and certified to CE and CSA standards:

**EMC:**

- EN IEC 61326-1: 2021(*): “Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements”
- EN 55011:2016 + A1:2017 + A11:2020 + A2:2021: "Industrial, scientific and medical equipment. Radio-frequency disturbance characteristics. Limits and methods of measurement."
- EN 61000-4-2:2009: "Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test."
- EN IEC 61000-4-3:2020: "Electromagnetic compatibility (EMC)- Part 4-3: Testing and measurement techniques- Radiated, radiofrequency, electromagnetic field immunity test."
- EN 61000-4-4:2012: "Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test."
- EN 61000-4-5:2014+A1:2017: "Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test."
- EN 61000-4-6:2014: "Electromagnetic compatibility (EMC) - Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields."
- EN 61000-4-8:2010: "Electromagnetic compatibility (EMC) - Part 4-8: Testing and measurement techniques - Power frequency magnetic field immunity test."
- EN IEC 61000-4-11:2020 + AC:2020-06 + AC:2022-10: "Electromagnetic compatibility (EMC) - Part 4-11: Testing and measurement techniques - Voltage dips, short interruptions and voltage variations immunity tests."

**Safety:**

- IEC 61010-1{ed3.0}b Safety Standard 2010-6 + AI:2019 + Ac:2019
- IEC 61010-2-030:2021 +Aii:2021 Particular requirements for T+M equipment

## *CS1300 Series Pods*

The CS1300 Pods are used to extend the capability of the CS548 oscilloscope. Two Pod connectors are provided on the CS548. Pods use LVDS communications capable of 400 Mbps for good noise immunity, low EMI, and reliability. These pods are available now:


1. **CS1301 Isolated digital inputs (2x included in standard delivery)**

   Two CS1301 pods are included with the CS548.
   The pod supports 4 isolated digital inputs with one common, and fixed voltage threshold of $V_{HI}$>2.3V, $V_{LO}$ <0.9 V, with +18, -15V overload protection.

   Isolation is 600$V_{RMS}$ Cat III (UL), or 800 $V_{DC}$ (VDE), based on an ISOW7844FDWE, and PCB creepage. Common mode rejection is 100V/ns.

2. **CS1302 Isolated digital outputs (optional accessory)**

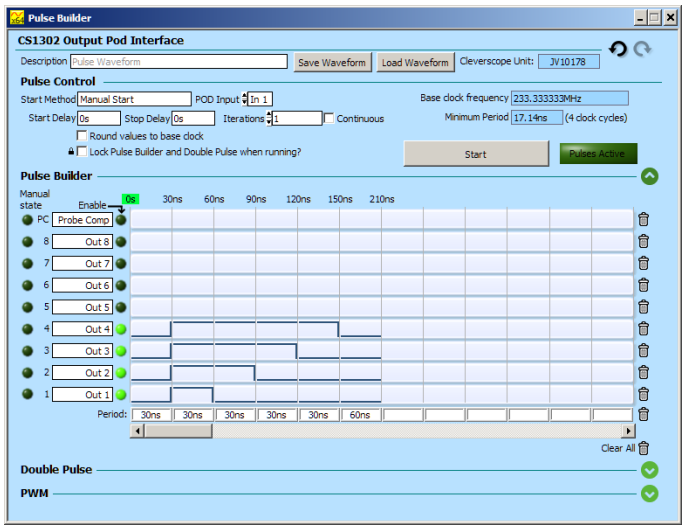
   The CS1302 is an optional purchase. The pod has 1 input, and 4 outputs, one of which may be assigned as a high speed clock. The pod allows high speed generation of arbitrary signals, optionally synched to the clock, with simultaneously recording of the input signal. It may also be used as a fast isolated SPI or UART port.
   The application supports arbitrary pulse generation, PWM, and double pulse testing using the CS1302.

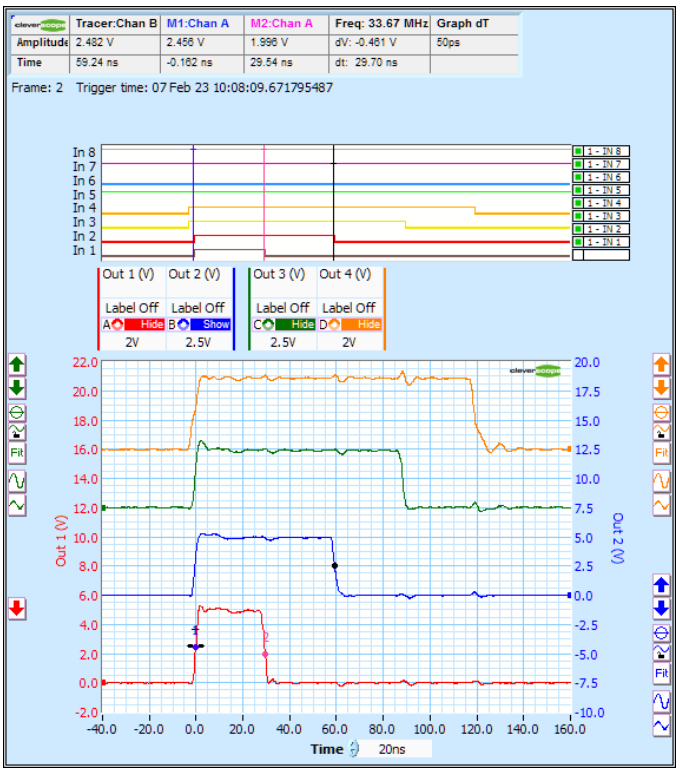

   The output level is 5V ($V_{SEL}$ open), or 3.3V ($V_{SEL}$ pulled low).

   Isolation is 600 $V_{RMS}$ Cat III (UL), or 800 $V_{DC}$ (VDE), based on an ISO7840DW and ISOW7744DFMR, and PCB creepage. Common mode rejection is 100V/ns.

## Pulse Builder

The CS1302 is supported by Pulse Builder in the Cleverscope4 application. Pulse Builder can be used to draw pulse trains, Double Pulse Test pulses, and PWM output with arbitrary durations between each edge:



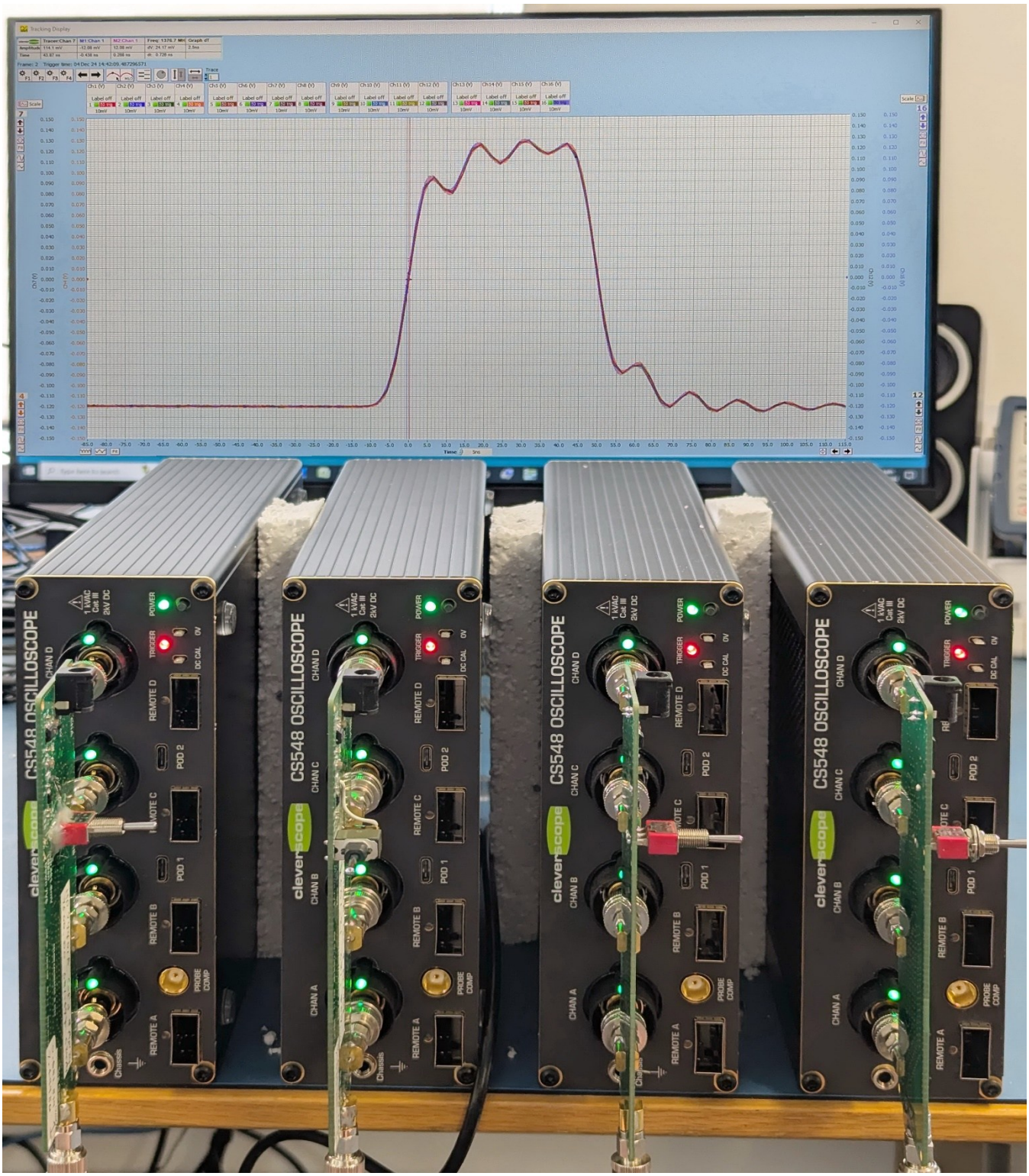




Here 4 pulses have been defined, and output via a CS1302. Outputs 1-3 are mirrored as Inputs 1-3. Input 4, which is a CS1302 input, is physically measuring Output 4. Pulses as short as 17ns can be generated using the CS1302. The incremental step resolution is 4.3 ns. These pulses are 30, 60, 90 and 120 ns long.

## Multi-Unit Capture

Up to 4 units may be connected using the CS1021 Link cables from a unit Link Out port to the next unit Link In port. Clock, trigger and control are shared via the link cables. Time alignment and amplitude matching are good. All 4 units perform as one 16 channel oscilloscope using the Cleverscope PC application.

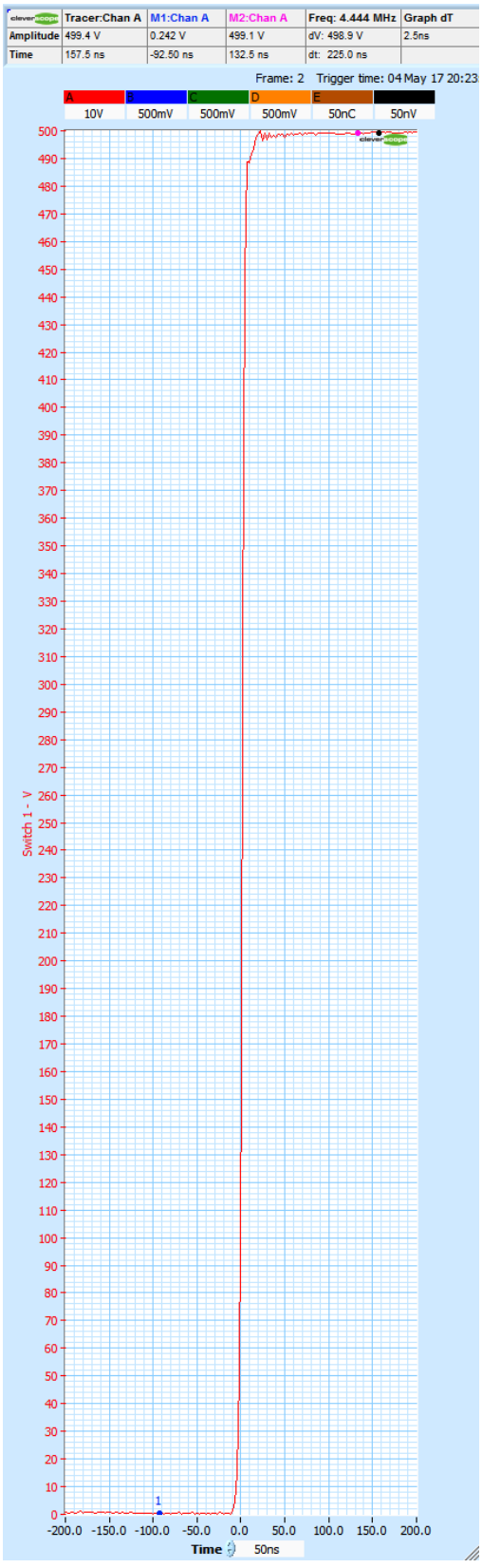
Here an unterminated 50ns pulse is displayed on all 16 channels using a 16 way time aligned signal splitter sourced from one units signal generator. The time axis is 5ns/div. Dispersion of about 700 ps is displayed between the two maker lines.



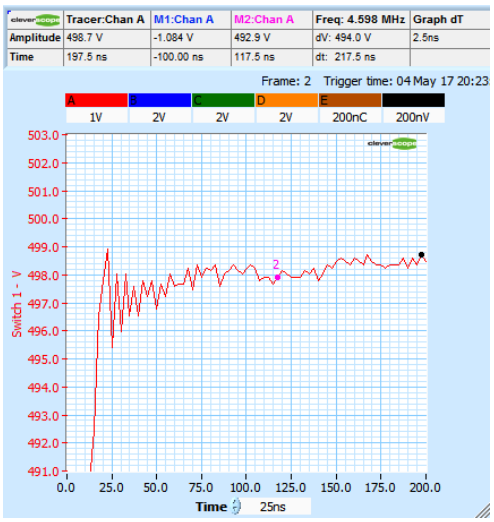
# Selected Measurements

## *Response to 500V 10ns transition*

We measure the CS1090 Switch 1 output (500 V, 10 ns rise time):




This trace shows the transition measured using a 100x probe. The display pixel resolution masks the actual channel resolution, shown here at 1 V/div:

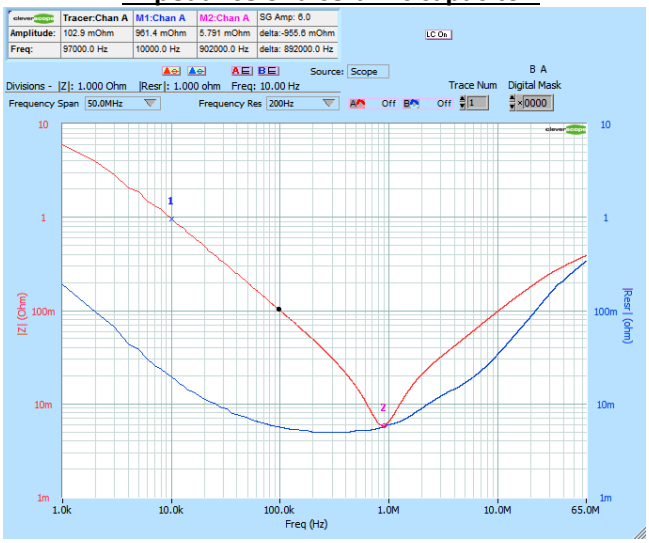



This kind of resolution is not possible with an 8 bit oscilloscope.

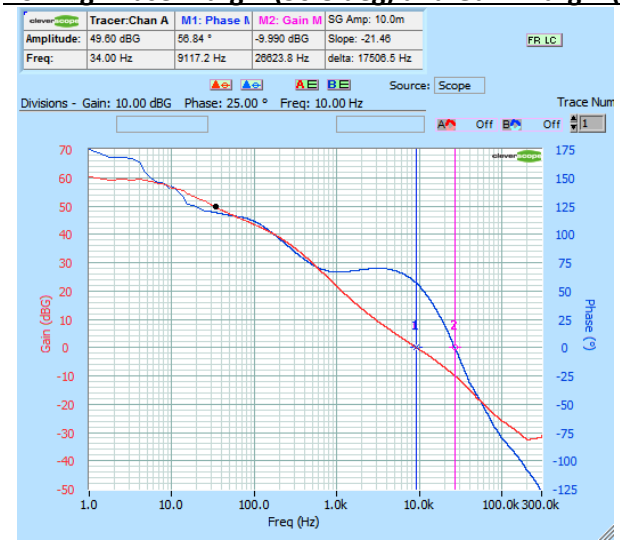
## *Frequency Response Analysis Functions (FRA)*

The Frequency Response Analysis (FRA) system uses the isolated signal generator to provide stimulus for component, system or power supply measurements. The measurements available are shown in the Displays/FRA section of the data sheet. Here are a collection of measurements made using the FRA system (zoom on the PDF to see the detail):

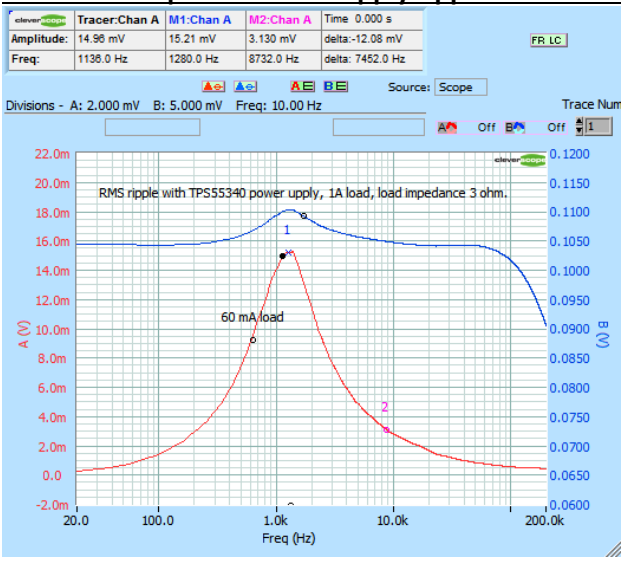
**Impedance of a ceramic capacitor:**




**PSU Gain Phase of switching power supply TPS55340 howing Phase Margin (56.8 deg) and Gain Margin (20 dB):**

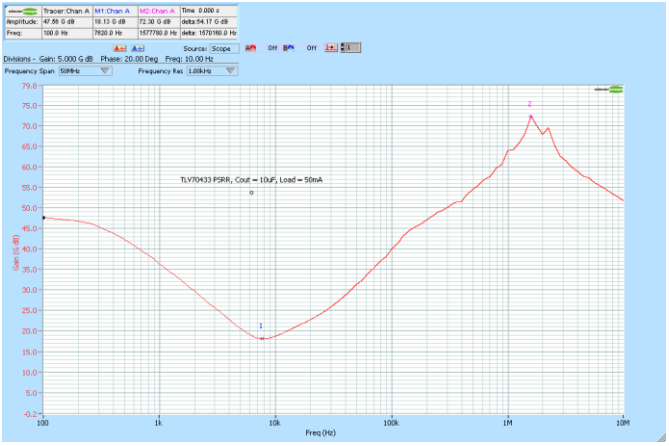



**PSU Shunt Impedance and supply ripple TPS55340:**




**Gain/Phase of a 10.7 MHz filter:**


**TLV70433 PSRR using CS1070 (1A 50 MHz Amplifier):**



**Powered LTC3589 Output Impedance using CS1070:**

# Cleverscope Application Specification

## Analog Inputs

Items marked with * still have to be implemented. See Specification Status section.

| Parameter | Specification | Notes |
|---|---|---|
| **Number of channels** | 0 - 4 | Fiber optic isolated from each other, local or remote digitizer. |
| **Isolation Voltage – Local** | 2 $kV_{DC}$, 1 $kV_{AC}$ CAT II, 600 $V_{AC}$ CAT III | Supported by IEC 61010-1 Ed 3.0 and IEC 61010-2-30 (Test Equipment) 22 mm creepage and 18 mm clearance, reinforced. |
| **Isolation Voltage – Remote Digitizer** | ±30 $kV_{DC}$ | When mounted >150 mm from reference plane or other structures not at the common mode voltage.<br>If measured common mode voltage frequency is >1 MHz, then must be mounted >1 m from any other conductive structure not at the common mode voltage. |
| **CMRR** | >120 dB at 1 MHz<br>>115 dB at 10 MHz<br>> 100 dB at 50 MHz | 20 dBV signal applied to coax common and earth reference 4 mm socket. |
| **ADC resolution** | 14 bits | |
| **Input Ranges** | ±0.8V with 100 µV resolution<br>±8 V with 1 mV resolution | Use probes to extend the range, e.g. 800 V with 100x probe. The application automatically scales all values to compensate for probe attenuation. |
| **DC voltage measurement accuracy** | < ±0.15 % of range maximum. | After self-calibration or calibration. |
| **Sample Rate** | 500 MSPS | All Analog and Digital channels simultaneously. |
| **Sample Memory** | 500 MSamples * (installed) | Currently 4 x simultaneous channels with 16 MSamples per channel. |
| **CM leakage to other channels** | < -125 dBc | 20 dBV signal to CM channel, measured on other channels whole bandwidth, ±0.8 V range |
| **Channel to Channel Skew** | < ±144 ps | Done using a 1 MHz coherent sine wave |
| **Cross talk at 10.7 and 30 MHz** | < -115 dBc | Using 1.6V p-p into the channel |
| **RMS Channel Noise 1 MSamples** | ~200 $\mu V_{RMS}$, ±0.8 V range<br>~ 2 $mV_{RMS}$, ±8 V range | Inputs open |
| **Pk-Pk Channel noise 1 MSamples** | 1.8 $mV_{p-p}$ for ±0.8 V range<br>15 $mV_{p-p}$ for ±8 V range | Inputs open |
| **Sample clock jitter** | 300 $fs_{RMS}$ | |
| **Sample clock Freq tolerance** | max ±2 ppm | At 25 °C |
| **Sample clock temp stability** | max ±0.5 ppm | Over -40 to +85 °C |
| **ENOB (rms)** | 11.6 bits, or 1 part in 3,300 | Inputs open |
| **Noise free bits** | 10.3 bits, or 1 part in 1300 | Inputs open |
| **Spectral Noise floor, no protrusions** | -100 dBV<br>-115 dBV | <2 MHz, 200 MHz BW, 1 kHz resolution<br>>2 MHz, 200 MHz BW, 1 kHz resolution |
| **Sinad** | > 64 dBc at 1 MHz<br>>63 dBc at 10 MHz<br>>55 dBc at 30 MHz | 1 $V_{p-p}$ into 50 Ω signal |
| **HD2+3** | < -80 dB at 1 MHz<br>< -76 dB at 10 MHz<br>< -71 dB at 30 MHz | 1 $V_{p-p}$ into 50 Ω signal |
| **THD** | < -76 dB at 1 MHz<br>< -74 dB at 10 MHz<br>< -67 dB at 30 MHz | 1 $V_{p-p}$ into 50 Ω signal |
| **Pulse Flatness** | <700 µV<br><2 mV<br><200 mV | 0.5 V pulse, 500 µs duration, ±0.8 V range<br>0.5 V pulse, 500 µs duration, ±8 V range<br>500 V pulse, 500 µs duration, 100x probe |
| **Overload recovery** | 4 ns | Recovery from 10x overload |
| **Maximum Differential Input Voltage** | ±1 kV, derated above 1 MHz | Derated at 20 dB/decade |
| **Maximum Common Mode Input Voltage** | ±2 kV, derated above 10 MHz | Derated at 20 dB/decade |
| **Spectral Flatness** | ±0.5 dB from DC - 160 MHz<br>-3 dB at 200 MHz | Supports 200 MHz Bandwidth |
| **Input Resistance** | 1 MΩ | DC resistance |
| **Input Capacitance** | 21 pF | Signal Input to Signal Common |
| **Isolation Capacitance** | 20 pF | Channel ground to chassis |

# Digital Inputs

| Parameter | Specification | Notes |
|---|---|---|
| **Number of inputs** | 8 | |
| **Common mode transient immunity** | 100 V/ns | |
| **Input threshold max** | 2.3 V rising, 0.9 V falling | Using CS1301 isolated probes (ISOW7844).<br>Using CS1300 threshold programmable 0-8 V |
| **Isolation capacitance** | <5 pF | To chassis ground, at 1 MHz |
| **Isolation operating voltage** | 880 $V_{DC}$ (600 $V_{AC\ rms}$)<br>1130 $V_{DC}$ | Re-inforced insulation, EN61010-1<br>Re-inforced insulation, CSA and IEC 60950-1 |
| **Maximum Data rate** | 100 Mbps | Sampled at 500 MSPS* (400 MSPS now). |
| **Propagation delay** | 13 ns (typ.) | Compensated for within CS548 |
| **Connectors** | POD1 (1..4) & POD2 (5..8) | Located on front panel, USB-type C physical connector (use with Cleverscope cables and accessories only). |
| **POD connector total output power** | 5V 1.5A | Current limit is total for both connectors, short circuit proof. |

# Signal Generator

| Parameter | Specification | Notes |
|---|---|---|
| **Output Frequency Range** | DC - 65 MHz | -3 dB at 65 MHz on unfiltered output |
| **Outputs** | Unfiltered, filtered | Unfiltered is used high slew rate signals (AWB or square wave). Filtered includes a reconstruction filter for minimum sample clock injection into the signal. |
| **CMRR** | >100 dB at 1 MHz<br>>95 dB at 10 MHz<br>>90 dB at 50 MHz | Limited by analog channels used for test.<br>The Sig Gen connection reduces CMRR by about 20 dB, if direct connected to a Channel. |
| **Common mode transient immunity** | 100 kV/µs | For control of the output DAC |
| **Isolation Voltage** | 600 $V_{DC}$, 300 $V_{AC}$ CAT II | Supported by IEC 61010-1 creepage and clearance, reinforced |
| **Unfiltered rise/fall time** | 3.2 ns | Full scale swing |
| **Sine Wave Flatness** | ±0.2 dB<br>+0.2 dB, -3 dB | 0 - 20 MHz filtered + unfiltered, 50 Ohm terminated<br>20 - 65 MHz unfiltered |
| **DAC Resolution** | 12 bits | |
| **NCO Resolution** | 24 bits | 10.7 Hz resolution at 180 MSPS |
| **Output amplitude** | ±1 mV to ±3.5 $V_{p-p}$ | Programmable 1 mV resolution, constrained to total range ±3.5 V including offset |
| **Output offset** | 0 to ±3.5 $V_{p-p}$ | Programmable, 1 mV resolution |
| **Output Noise** | < 100 $\mu V_{RMS}$ | |
| **SFDR** | > 84 dBc | At 10 MHz |
| **IMD** | > 88 dBc | At 10 MHz |
| **HD2+3** | < -77 dBc | At 10 MHz |
| **Arb Waveform Memory** | 4 kSamples * | Using AD9102 - UI to be implemented still |
| **Sample Rate** | 180 Msps | Programmable Sample rate 1 sps - 180 Msps |
| **Frequency list values** | 2 k * | Frequency list output in response to trigger |
| **Envelope can be amplitude modulated** | Yes * | |
| **Pattern Generator** | Yes * | Start period, output period, stop period, pattern repeat count. |
| **Trigger** | Input from FPGA * | FPGA may trigger a pattern based on Channel Trigger or other event. |

# USB

| Parameter | Specification | Notes |
|---|---|---|
| **Supported Modes** | USB 2.0 and USB 3.0 | USB 2.0 @480 Mbit/sec and USB 3.0 at 5 Gbps |
| **Throughput** | 30 Mbps and 130 Mbps | |
| **Connector** | USB-C | Plug is reversible. No output power. |
| **Protection** | Common mode choke + ESD diodes | Using ECMF04-4HSWM10 |
| **Indicators** | USB on and correctly connected | Power of signal is indicated by LED off. |

# Ethernet *

| Parameter | Specification | Notes |
|---|---|---|
| **Connection method** | Small Form factor Pluggable module (SFP) | An SFP socket is provided for use with an SFP module. Either an optical or a copper connected SFP module will be supplied based on the order.<br>SFP socket supplies 3.3V 150 mA for module.<br>No PoE available. |
| **Wired Supported Modes** | Ethernet 10/100/1000 * | Using an RJ45 Ethernet socket connected copper SFP module. Transformer based isolation.<br>Software being implemented |
| **Optical supported mode** | Ethernet 1000BASE-LX * | Gigabit (1G) Ethernet using an LC fibre cable connected optical module. Full optical isolation.<br>Software being implemented |
| **Throughput** | 12 MBps and 120 MBps | |
| **Connector** | SFP Socket | Small Form Factor Pluggable socket |
| **Indicators** | Ethernet on and correctly connected | Power of signal is indicated by LED off. |

# Power Supply

| Parameter | Specification | Notes |
|---|---|---|
| **Input Voltage Range** | 10 - 24 DC | Over voltage protected |
| **Power consumption** | 43 W | |
| **Connector** | Barrel Socket, 2.5mm I.D. x 5.5mm O.D | Connection is reverse polarity protected. |
| **Protection** | Clamped to +68 V<br>Clamped to -32 V<br>Operates with 35 V<br>Survives with 5 V | ISO16750 pulse A (79 Ohm 0.5 Ohm)<br>ISO7637 Pulse 1 (-600 V, 50 Ohm)<br><br>FPGA operation at 5 V, ADC operational at 7 V. |
| **Indicators** | Power On, Channel Status | Software controlled. |
| **Power Adaptor** | VEC65US19 | 100 - 240 $V_{AC}$ input, 19 $V_{DC}$ 65 W output. |

# Digital Port *

The Digital Port is based on a programmable logic IC, and can be used for generating complex state based sequences or reacting to a complex set of inputs. The port includes triggering capability. The UI has not been completed.

| Parameter | Specification | Notes |
|---|---|---|
| **Input/Outputs** | 16 | Programmable as In or Out |
| **Logic Level** | Programmable 1.8 - 5 V | All I/O operate at the same logic level |
| **Control IC** | SilegoSLG46826V | User configurable programmable logic with analog functions |
| **Resources** | 19 Multi-function Macrocells<br>Prog Oscillator, 25 MHz, 2 MHz, and 2 kHz.<br>256x8 EEPROM<br>4 Analog Comparators<br>2 x Deglitch filters<br>Two voltage references<br>I2C port | 2-4 bit for complex logic<br>All resources can be arbitrarily connected as required. |
| **Programming** | Silego GP Designer | Visual schematic designer of circuit functions downloaded into CS548 |
| **Trigger In/Out** | Bidirectional Trigger | For interaction with measurement system. |
| **Protection** | | Over voltage protection to +12 V and -6 V |
| **Connector** | WE 61202021721 | 20 pin 0.1” double row |
| **Output power** | Variable 2.5-5.0 V, 1 A | Short circuit proof. |

# Link Port *

The Link Port is used for controlling Cleverscope accessory devices such as the CS1070 1 A 50 MHz power amplifier, and the CS1113 $V_{CE}$ Sat Probe. It also includes RS232, SPI and $I^2C$ ports for controlling user equipment.

| Parameter | Specification | Notes |
|---|---|---|
| **Digital Port Use** | 2 Digital In, 4 Digital Out | Used for accessory control |
| **I2C Port** | 400 pbps port | For control of user devices |
| **SPI Port** | 1 MHz SPI Port | For control of user device, mutually exclusive with RS232 Port |
| **RS232/RS422 Port** | 3 V level RS232 port, or differential RS422 port, programmable baud rate | For control of user device, mutually exclusive with SPI Port |
| **Trigger Port** | Trigger In/Out and control | |
| **Protection** | | Over voltage and reverse voltage protection using ESD devices |
| **Connector** | Mini Din 8 | |
| **Output Power** | 5 V, 1.5 A (current limited) | Pin 1 = 5 V, Pin 2 = GND. |

# Link In/Out Port

The Link In/Out Port is used daisy chaining 2, 3 or 4 CS548 Cleverscopes.

| Parameter | Specification | Notes |
|---|---|---|
| **Clock ports** | Reference clock, 500 kHz | The last CS548 in the chain provides the 500 kHz reference clock that is used for simultaneous sampling by all units. |
| **Trigger Ports** | Trigger transfer | The Trigger Ports transfer the trigger to other units. |
| **Control Ports** | Control signals | The control signals are used to signal readiness to trigger, and sampling state. |
| **Connectors** | HDMI | Use with 500mm linking cable supplied by Cleverscope. Only use Cleverscope approved cables. |
| **Output Power** | 5 V 1.5 A (current limited) | Only available on LINK OUT. |

# Probe Compensator Output

The probe Compensator output is used to compensate the probe response for time domain flatness.

| Parameter | Specification | Notes |
|---|---|---|
| **Signal** | 1 kHz Square Wave | Variable 50mHz to 58.3 MHz |
| **Duty Cycle** | 50% | Variable with 8.6 ns resolution to 10 s high. |
| **Amplitude** | Programmable 5 - 12 V | 150 mA current limit |
| **Rise/ Fall Time** | ~ 1 ns | |
| **Connection** | BNC, 50 Ω source | Designed for 10x probe. 10 mV dip with 50 Ω load. |

# Environmental

| Parameter | Specification | Notes |
|---|---|---|
| **Temperature** | 0 °C to +40 °C<br>-20 °C to +60 °C | Operating<br>Storage |
| **Cooling Method** | Fan Assisted | |
| **Humidity** | 0 °C to +40 °C<br>>40 °C | <90 % relative humidity<br><60 % relative humidity |
| **Altitude** | <3,000 m<br>15,000 m | Operating<br>Non-operating |

# Mechanical

| Parameter | Specification | Notes |
|---|---|---|
| **Size** | Height 69 mm<br>Width 187 mm<br>Length 280 mm | Including feet<br><br>Including connectors |
| **Weight (approx.)** | 2.8 kg<br>4.1 kg | Acquisition Unit only<br>Complete in display box |
| **Material** | Anodized Aluminium | |

## Calibration

| | |
|---|---|
| **Calibration method** | Automatic self-calibration |
| **Calibration Voltage Source (inside each channel)** | 2.5 V reference, 40 ppm stability (1000 Hrs), 30 ppm/°C |
| **Calibration Voltage Source (on DC Cal. pins)** | 7.5 V reference, 20 ppm stability, ±0.035 % accuracy, 7 ppm/°C |

## Displays

| | |
|---|---|
| **Windows** | Simultaneous Capture, Tracking, Spectrum, Information, Maths, XY, Control Panel, Streaming, Frequency Response Analysis (FRA), Pulse Builder and Protocol setup windows |
| **Scope window functions** | Defines capture specification for signal acquisition unit, defining amount of time before trigger, amount of time after the trigger, lower amplitude limit, upper amplitude limit.<br>Defines Tracking graph time position, when tracking graph is linked.<br>Defines trigger level and direction<br>Full zoom and Pan in both axis.<br>Annotations.<br>Custom units<br>Custom colours |
| **Tracking window functions** | Displays zoomed section of captured signal. Resolution from 1 ns to 5 s/div.<br>Full zoom and Pan in both axis.<br>Annotations.<br>Custom colours |
| **Spectrum window functions** | Display spectrum of signal captured in capture window.<br>User definable resolution<br>Full zoom and Pan in both axis.<br>Annotations.<br>Custom units<br>Custom colours |
| **Maths window function** | Displays results of Maths equations.<br>Maths equations are user entered expressions involving any of the inputs (analog and digital), previous maths equation line results, and an arbitrary number of function results (+ - * / sqrt, power, log, ln, all transcendental functions, equality functions).<br>Custom units.<br>Provide live Matlab link. |
| **XY window function** | Displays XY graph from source (Capture, tracking, spectrum, or Maths |
| **Information window functions** | Displays automated measurements (see below)<br>Used to log derived information values to disk, with a period of between 0.05 – 86,400 secs per sample.<br>Live logging to Excel<br>DDE live value transfer to Excel. |
| **Control window functions** | Provides Trigger settings – analog and digital<br>Provides Sample control – single, triggered or automatic.<br>Provides access to tools – Pan, Zoom, Annotate<br>Controls Frame store<br>Controls Spectrum resolution, acquisition method and averaging |
| **Frequency Response Analysis (FRA)** | FRA control panel is used to setup up oscilloscope/signal generator to make automated measurements of these values vs frequency:<br>• RMS Amplitude<br>• Power<br>• Power Density<br>• Gain/Phase<br>• Impedance + $R_{ESR}$ or Q/D Factor or Phase<br>• Capacitance + $R_{ESR}$ or D Factor or Phase<br>• Inductance + $R_{ESR}$ or Q Factor or Phase<br>• Shunt Impedance (magnitude without phase for low impedances)<br>• PSU Gain/Phase - for finding Gain/Phase of powered up power supplies<br>• PSU PSRR - for finding PSRR of powered up power supplies<br>• PSU Output Impedance - for finding Output Impedance of powered up power supplies<br>• PSU Input Impedance - for finding Input Impedance of powered up power supplies<br>• Probe calibration functions for maximum accuracy. |
| **Protocol Setup** | Provides protocol setup for I2C, SPI, UART and parallel bus. |
| **Pulse Builder** | Allows manual control of isolated digital outputs state, Pulse Builder for pulse trains, PWM with up to 4 PWM generators, including single output, half bridge, or full bridge, and double pulse test for high side and low side. |

## Measurements

| | |
|---|---|
| **Cursors** | Voltage Difference between cursors<br>Time difference between cursors<br>Reciprocal of ΔT in Hertz (1/ΔT). |
| **Automated measurements** | <table><tr><th>Function</th><th>Function</th><th>Function</th><th>Function</th></tr><tr><td>DC</td><td>0 -> 1 Time</td><td>DC</td><td>A at F</td></tr><tr><td>RMS</td><td>1 -> 0 Time</td><td>RMS</td><td>B at F</td></tr><tr><td>Max</td><td>V '1'</td><td>Fsignal</td><td>A max</td></tr><tr><td>Min</td><td>V '0'</td><td>Vsignal</td><td>A min</td></tr><tr><td>Pk-Pk</td><td>V swing</td><td>F1</td><td>B max</td></tr><tr><td>Std Dev</td><td>Overshoot</td><td>V1</td><td>B min</td></tr><tr><td>Period</td><td>Slew rate</td><td>F2</td><td>Amax at 0 B</td></tr><tr><td>Fundamental Frequency</td><td>Pulse Period</td><td>V2</td><td>Amin at 0 B</td></tr><tr><td>Fundamental Peak amp</td><td>Pulse Frequency</td><td>F3</td><td>Bmax at 0 A</td></tr><tr><td>Pulse Length</td><td>Pulse Length</td><td>V3</td><td>Bmin at 0 A</td></tr><tr><td>Duty Cycle</td><td>Duty Cycle</td><td>SINAD</td><td>A -3dB L: H</td></tr><tr><td></td><td></td><td>THD</td><td>B -3dB L: H</td></tr><tr><td></td><td></td><td>HD2+3</td><td></td></tr></table> |
| **Custom units** | 6 characters |
| **Custom signal names** | 20 characters |
| **Custom scaling** | Scale + offset by defining two ($V_{IN}$, $V_{OUT}$) points |
| **User definable colours** | Signals, Background, Major Grid, Minor Grid |

## Mathematical Functions

| | |
|---|---|
| **Functions over the signal** | Differentiation, Integration, Filtering, Power functions, Matlab interface, Signal Processing functions |
| **Functions on a data point** | Addition, subtraction, multiplication, division, squaring, square root, (inverse) sine, cosine, tangent, tangent, log, sign etc. Equality operations. |
| **Maximum number of sequential mathematical equations** | 10, symbolic with multiple operators and operands. |

## Spectrum Analysis

| | |
|---|---|
| **Frequency Range** | User definable, Range = 0- 1/Scope Graph ΔT<br>Frequency axis – log or linear. |
| **Analysis Output** | RMS Amplitude, Power, Power Density, Gain/Phase |
| **Frequency Resolution** | In 1, 2, 2.5, 5 sequence with 1 part in 1M resolution. |
| **Output type** | Volts, Power, Gain/Phase in linear, dB, degree or radian values. Impedance, LCR, Q and DF. Custom units can be applied. |
| **Window types** | None, Hanning, Hamming, Blackman-Harris, Flat top, Low Sidelobe |
| **Averaging** | Moving average, block average, peak hold. |
| **Averaging method** | Vector averaging in time domain if triggered.<br>RMS averaging in frequency domain if not triggered. |

## Protocol Decode

| | |
|---|---|
| Protocols | I2C, SPI, UART and parallel bus. |
| Protocol decode inputs | Digital Inputs 1-8, External trigger, Channels A, B<br>User defined threshold when using analog inputs |
| Protocol decode variables | Number of bits, Clock edge rising or falling, Bit invert/non-Invert, Select Hi/Lo, MSB first or not, Number of stop bits. |
| Output display type | Naming label. Character, Hexadecimal or Decimal Number. Colour. |

## *Streaming*

| | |
|---|---|
| Sampling Rate | 12 SPS – 3 MSPS (Streaming rate will be improved in the future) |
| Sample preparation | Peak capture or Filter prior to decimation. Using 10 MHz filter with 14 bit ADC we achieve 13 bits ENOB at 3 MSPS (60 µV noise floor with ±0.8 V range). |
| Sample storage | Up to 500 Gsamples. Samples are stored in multiple smaller files to increase speed. |
| Review capabilities | Zoom and pan anywhere in sample space. Samples are displayed peak captured (i.e. 1µs pulse will still be visible in 1 day long sample record). |
| Export capabilities | Export tab delimited text, binary, or Cleverscope format file. Output between markers, or current display. Set output depth. |

## *Data Export*

| | |
|---|---|
| **File types output** | Cleverscope proprietary, Tab delimited text (Excel compatible), Excel file (for signal information logging), binary (format given in help). |
| **Live Data output** | DDE to Excel, direct placement of data into live Excel sheet<br>Live data output to and return from Matlab |

## *Windows facilities*

| | |
|---|---|
| **Standard Functions** | Copy and Paste<br>Save and Open native format (saves full setup)<br>Save and Open tab delimited text file<br>Save and Open binary file (start time, dt, data)<br>Print with Date/Time, File Name and Description.<br>Print Setup |
| **Windows** | Dynamically resized<br>Can be placed anywhere on desktop<br>Can be docked to move with Cleverscope Control Panel<br>Can be docked to minimize/restore with one click. |
| **User defined units** | 6 characters |
| **User defined signal names** | 20 characters |
| **User defined scaling** | Scale + offset by defining two ($V_{IN}$, $V_{OUT}$) points |
| **User definable colours** | Signals, Background, Major Grid, Minor Grid |

Notes:

* Where a feature has not been implemented yet, it includes an asterisk * in the tables above.

# Specification Status

The CS548 is FPGA based, and upgradeable in the field. The customer can use Cleverscope ROM Loader to download new firmware and logicware to improve or add functions to the unit. The hardware system for the CS548 has been thoroughly tested to meet the specifications above and includes all the resources needed to meet the full specification. However, some software functions are still to be added. As these are added, updates are placed on our website for download at no cost. Cleverscope has used this method for years to add features such as FRA, streaming, complex maths etc. Should the current specification set meet your needs, you are able to use the CS548 now, and upgrade, at no cost, as further functionality becomes available.

Implemented in newer versions:

| Feature | Specification | Note |
|---|---|---|
| **Sampling Rate** | 500 MSPS | Implemented for units using an AD9690 ADC (Serial numbers IW10210 and later). Not for CS448. |
| **Sample Memory** | 128M Samples. | Organized as two 16M frames per channel for 4 concurrent channels (64M samples). Will be improved in the near future. |
| **Multi-unit Linking** | Up to four units can be linked via Link In and Link Out Ports | See page 8 Multi Unit Linking. Currently only CS548. |

Key features that still have to be implemented are:

| Feature | Specification | Note |
|---|---|---|
| **I/O Interfaces** | Ethernet is supported | Ethernet is currently not supported. We have implemented a hardware based IP stack, which is functional. Integration is proceeding with the CS548 firmware. |
| **Signal Generator Waveforms** | The signal generator will support AWB | The isolated Signal Generator currently only supports Sine and variable duty cycle Square wave generation and sweeping. The hardware (based on the AD9102) can generate 4K Arbitrary Waveforms, and patterns. The sig gen design includes a swept clock source to allow sweeping arbitrary waveforms (including square and triangle waves). The user interface for this is not yet done. |
| **Link Port** | The Link includes SPI, UART and I2C generation | The Link Port includes the facilities to generate I2C, Uart and SPI messages, as well as digital outputs. This capability is already supported by the firmware and DLL driver. However, a UI has not been implemented in the application. This will be done as time permits. The Link Port is used with I2C for CS1124 and CS1133 expansion. |
| **Faster Peak Capture** | Replay Peak Capture to run at close to real time | The current system has real time peak capture where the decimator outputs samples at below the maximum sample rate (eg Streaming). However, the replay peak capture system, while working, is not optimized and relatively slow. A DMA/Hardware based system will be used for peak capture replay. |
| **Digital Port** | Full use of SilegoSLG46826V | Hardware has been tested. The Silego programmer can be used. The CS548 will provide Silego design download at some point. |

# Standard Scope of Delivery

Not all needed accessories might be included in the Scope of Delivery. Please select them from the optional accessories list further below.

| | |
|---|---|
| **CS1001** | One piece per analog channel: 1x/10x analog probe,<br>±8 V / ± 80 V measurement ranges, 250 MHz, 600 V, 10 MΩ |
| **Common Mode Choke** | One piece per analog channel |
| **CS1301-1** | Isolated Digital Input Pod 1, Input 1-4 |
| **CS1301-2** | Isolated Digital Input Pod 2, Input 5-8 |
| **USB-Cable** | USB-C to USB-A type cable for PC connection |
| **Power Supply** | 19 V power supply for CS5x8 |
| **SMA-BNC Adapter** | Adapter for Signal Generator Output |
| **Ethernet Module** | Copper or Fiber wired, depending on selection |
| **100x or 200 x probe** | One per channel. Model depending on selection |


# Ordering Guide

Please choose you preferred equipment to configure your specific Cleverscope system. The steps 1 to 3 are mandatory, and the steps 4 to 7 are optional.

## Step 1: Choose your Cleverscope channel configuration

| | |
|---|---|
| **CS548** | 4 isolated analog channels, 4 remote connectors |
| **CS538** | 3 isolated analog channels, 4 remote connectors |
| **CS528** | 2 isolated analog channels, 4 remote connectors |
| **CS518** | 1 isolated analog channels, 4 remote connectors |
| **CS508** | 0 isolated analog channels, 4 remote connectors |


## Step 2: Choose your included probes (One piece per channel of selected type comes as standard)

The other probe can be ordered separately

| | |
|---|---|
| **CS1002** | Analog Probe 100x, ±800 V range, 250 MHz, 1.5 $kV_{RMS}$, 100 MΩ, 1.3 m |
| **CS1008** | Analog Probe 200x, ±1.6 kV range, 300 MHz, 1.5$kV_{RMS}$, 100 MΩ, 1.3 m |

## Step 3: Choose your included ethernet module (one module comes as standard)

The other module can be ordered separately

| | |
|---|---|
| **CS1042** | 1000BASE-T Copper SFP Transceiver |
| **CS1043** | 2.125 Gb/s Fibre SFP Transceiver |

## Step 4: Select your Remote Digitizers (Optional)

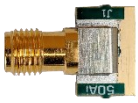
The 3 meter fiber is included in scope of delivery for each Remote Digitizer. If other fiber lengths is desired, please specify which length in your order from the table below.

**Remote Digitizers**

| | |
|---|---|
| **CS1200** | Active Optical Fibre isolated voltage digitizer, ±800 mV / ±8 V ranges, 200 MHz, 30 kV isolation, 100 dB CMRR @ 50 MHz, 14 bit ADC, 2 pF. Use probes to extend dynamic range as in internal channels. |
| **CS1201** | Active Optical Fibre isolated current digitizer, ±63A / ±630 A ranges, 200 MHz, 30 kV isolation, 100 dB CMRR @ 50 MHz, 14 bit ADC, 2 pF, one piece of CS1501 current shunt included. |

**Special Remote Digitizers Accessories**

| | |
|---|---|
| **CS1501** | Current Shunt for CS1201: 1 mΩ Shunt (only works with CS1201 digitizer) |
| **CS1026-1** | 1 meter Fiber cable for CS12XX devices |
| **CS1026-5** | 5 meter Fiber cable for CS12XX devices |
| **CS1026-10** | 10 meter Fiber cable for CS12XX devices |
| **CS1026-20** | 20 meter Fiber cable for CS12XX devices |
| **CS1026-30** | 30 meter Fiber cable for CS12XX devices |



## Step 5: Select Digital Pods Accessories (Optional)

**CS1302** Isolated digital I/O pod for generating up to 4 outputs for double pulse, half or full bridge PWM control or arbitrary pulse sequences. It includes one input and can be used to make an isolated SPI or UART pod. Pulse Builder supported.

**CS1308** [+] Fiber isolated digital input pod for measuring logic signals. Fibers bought separately

**CS1309** [+] Fiber Isolated digital I/O pod for generating up to 4 outputs for double pulse, half or full bridge PWM control or arbitrary pulse sequences. It includes one input and can be used to make an isolated SPI or UART pod. Pulse Builder supported. Fibers bought separately

**CS1027-1** 1 meter VersaLink Fiber cable for CS1308 and CS1309

**CS1027-10** 10 meter VersaLink Fiber cable for CS1308 and CS1309

Notes:
[+] CS1027-1 or CS1027-10 needed for operation.

## Step 6: Select further CS548 Accessories (Optional)

**CS1133** $V_{SAT}$ probe, clips at 150 mV, 1.5 V and 15 V to allow isolated measurement of transistor $V_{CEsat}$ while $V_{CE}$ swings up to 3300 V. Includes isolated power and control Link cable to CS548.

**CS1124** The CS1124 is used to expand the CS5x8 link port to serve up to 4 linked devices.

**CS1021** CS548 Link Cable for Link Out & Link In. Connect two, three or four CS548 for an eight, twelve or sixteen channel scope (for multi-scope synchronization: only use Cleverscope approved cables)

**CS1070** Power Amplifier, 50 MHz bandwidth, 36V p-p swing, including asymmetrical (e.g. +/-18V to +31V/-5V). Fixed 10x gain (20dB). Low noise (21nV/rtHz output noise), 1A drive current, Low distortion (-91dBc/-74 dBc at 1MHz 20Vp-p), low drift (40uV/deg C) Supplied with 19V 5A power supply and coax cable accessories. Internal negative rail generator to simplify input power requirements. Link Port controls power.

**CS1102** CS548 FRA Test fixtures - A set of three boards, low impedance (1 mΩ – 1 kΩ), high impedance (1 Ω - 25kΩ), and transformer testing (B-H, X primary, X leakage, Cww, N, and Xmutual).

## Step 7: Select Demo Accessory (Optional)

**CS1097** GaN Double Pulse Demonstration Board, 40-70 V, 150 A, access to all nodes. Includes 3 x CS1501. Requires CS1302 to operate and CS1201 to measure current. Optionally CS1133 to measure on-voltage.

## Notes

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